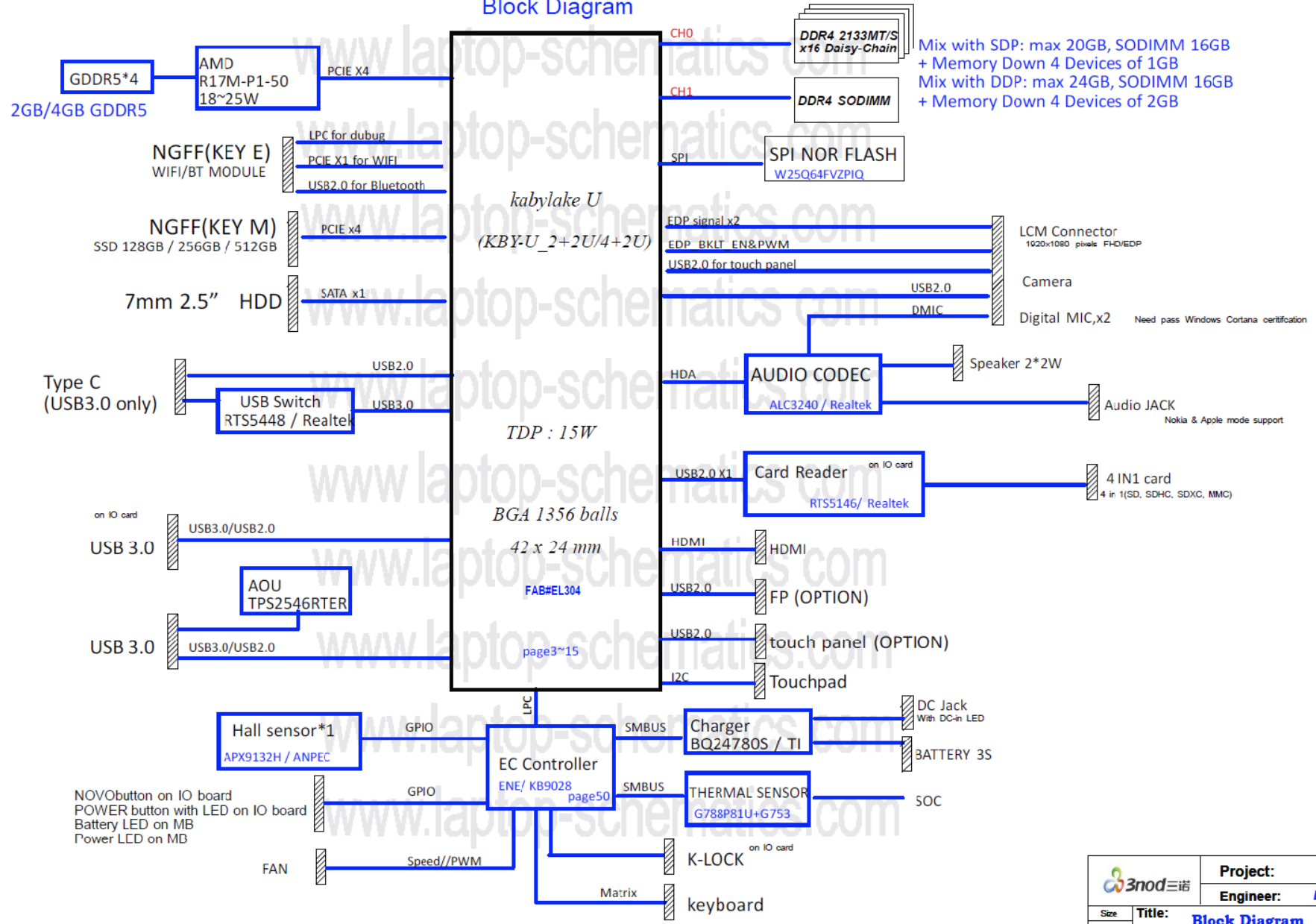


330S-KBL Series Block Diagram



		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: Block Diagram	Rev	
Custom		V01	
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05--SKL-U(3/12)SPI,ESPI,SMB,LPC	35 -- NC_HDMI CONNECTOR	65--PWR--+1.8V_Prim
06--SKL-U(4/12)HDA,EMMC,SD	36 -- DISPLAY	66--PWR-CPU_VR_IC
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15--SOC (DECOUPLING)	45 -- MICRO SIM	
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19--DDR4_CHA	49 -- DC JACK	
20--DDR4_CHB SODIMM	50 -- EMBEDDED CONTROLLER	
21--DDR4_Decoupling	51 -- BUTTON & LED	
22--NA	52 -- TYPE-C MULTIPLEXER	
23--RF / EMC Solution	53 -- TYPE-C PD CONTROLLER	
24 -- SYSTEM FLASH	54 -- NC TYPE-C BOOST VR	
25 -- NC EMMC	55 -- TYPE-C CONNECTOR	
26 -- PCIE SSD MODULE	56 -- UART CONN & HOLE & CLIP	
27 -- NC_MICRO-SD CARD	57 -- HW Change list	
28 -- NC_SD CARD POWER	58--PWR_DCIN/BATT CONN	
29 -- CPU THERMAL SENSOR	59--PWR_CHARGER(OZ8690)	
30 -- FAN conn	60--PWR--V5P0A / +V3P3A	

INTERNAL ONLY

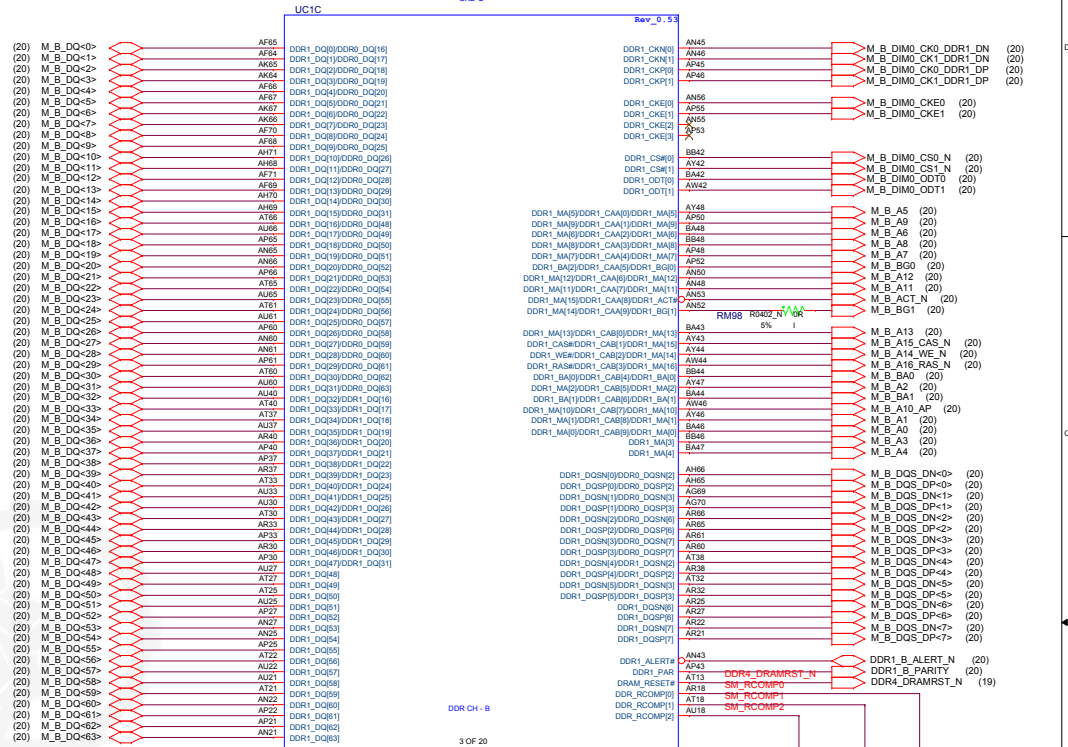
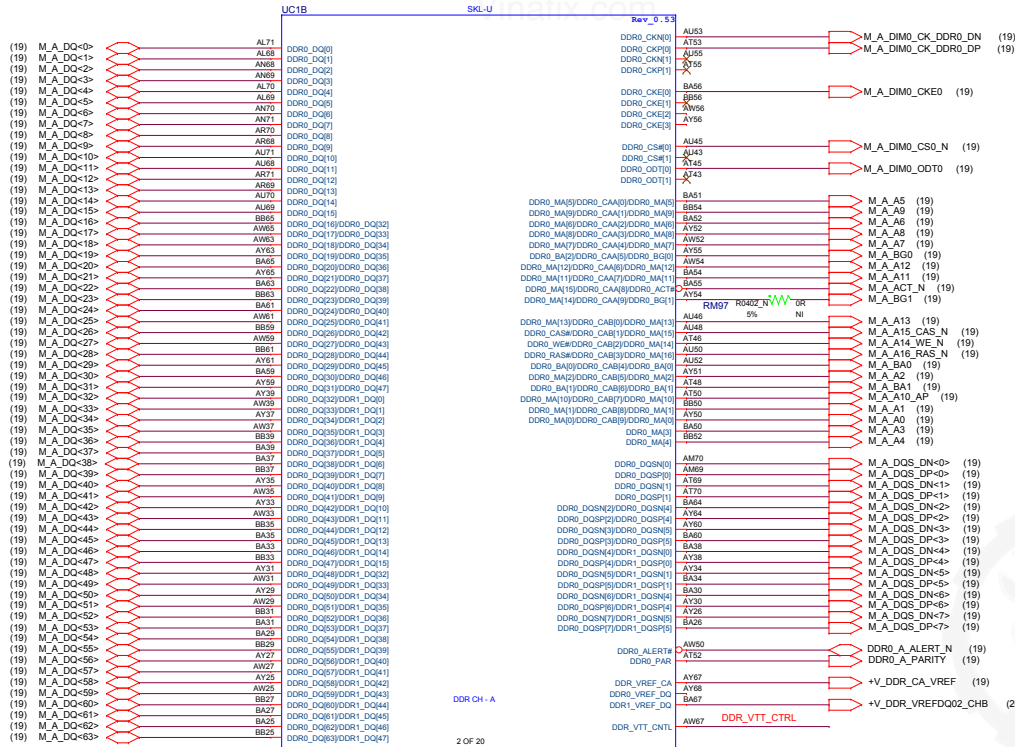
BPAGE DRAWING

shy_j_rml_...
Wed Jun 03 11:22:42 2015

		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title:	Rev	
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Interleaved

Interleaved



SKL-U_BGA1356

<BOM Structure>

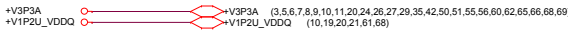
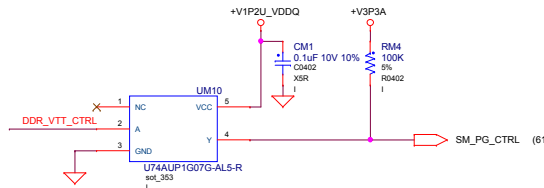
SKL-U_BGA1356

<BOM Structure>

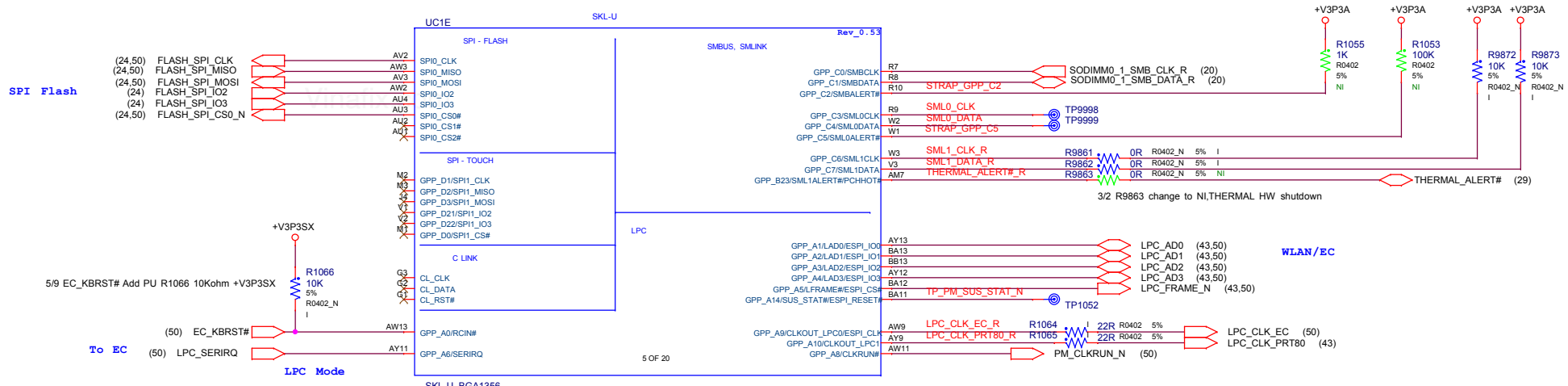
1. To support DDP, need to change two pins on DRAM. You have reserved them. Pls install the BOM.

DRAM M9 pin	X16 SDP	X16 DDP TwinDie
DRAM E9 pin	VSS	Connect to CPU BG1
	VSS	UZQ

	Default	
Memory size	4Gb or 8Gb	16Gb
DRAM M9 pin	RM95, RM96, RM97, RM98 need install	RM95, RM96, RM97, RM98 need install
DRAM E9 pin	RM99, RM100 need install	RM99, RM100 need install
SOC RCOMP0	RM3 121 ohm need install	



Project:		330S-KBL Series
Engineer:		Luffy
Size	Title:	KBL-U(2/12)DDR4
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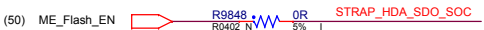
5/9 Page50 EC pin24 BAT_CHGOK_LED_N change to EC_KBRST#, connect to SOC pin AW13(RCIN)

- +V3P3A (3,4,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
- +V3P3SX (6,7,8,9,10,20,25,26,27,28,30,35,36,43,46,50,52)

SPIO_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPIO_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPIO_I02	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPIO_I03	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

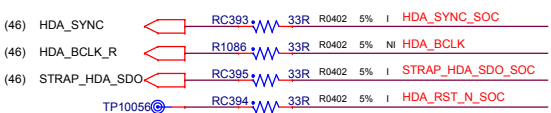
To Enable ME Override



Difference with armour
Add EC to enable ME override
5/23 R9848 install BIOS request

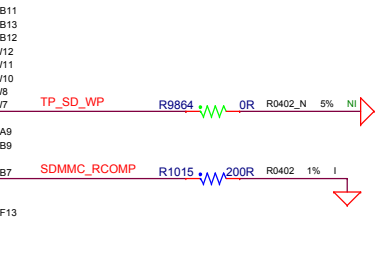
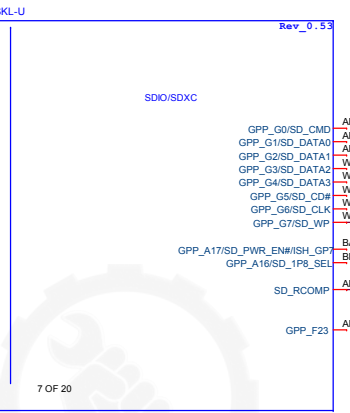
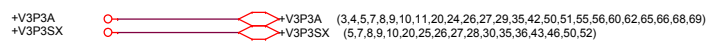
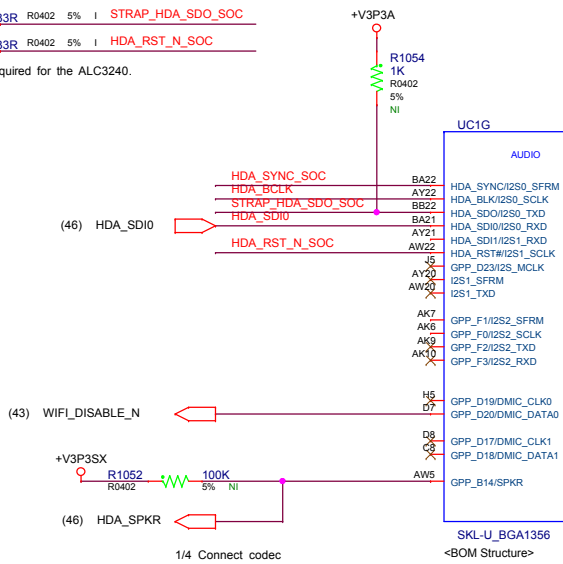
HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after PLTRST# de- asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
----------------------	---	-----------------------------	---

SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap. Notes: 1. The internal pull-down is disabled after PLTRST# de- asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
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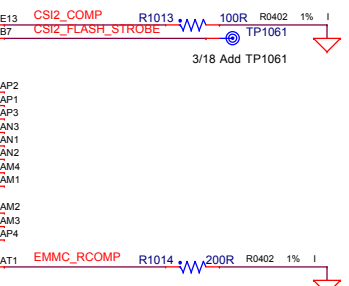
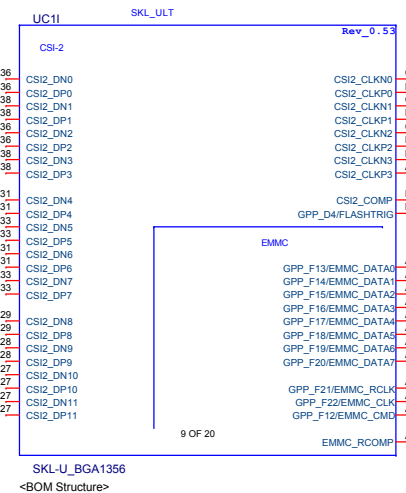
Note: RESET# is not required for the ALC3240.

HDA for AUDIO

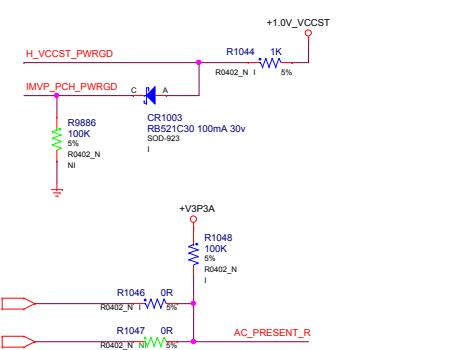
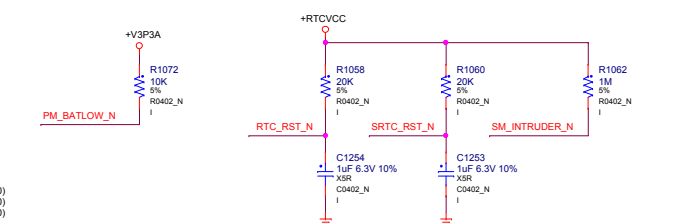
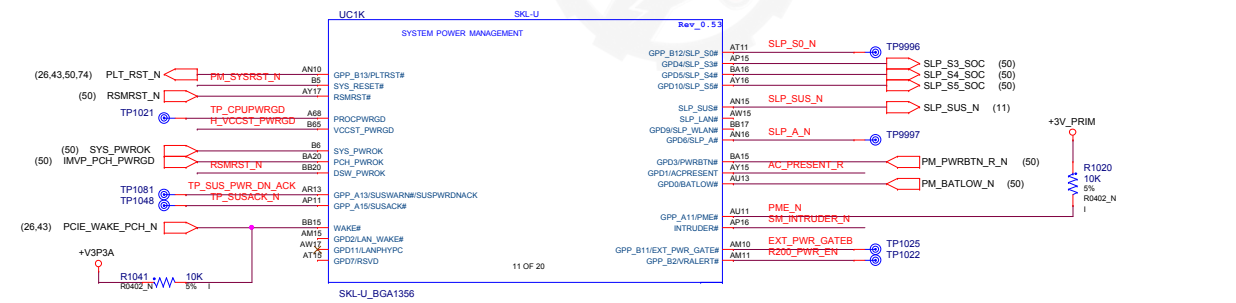
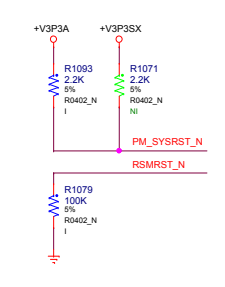
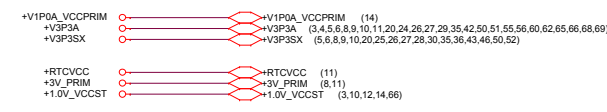
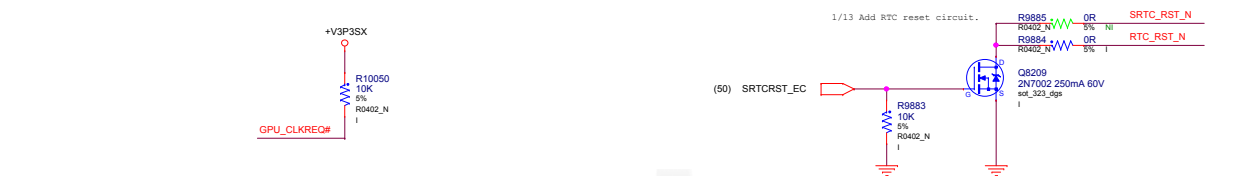
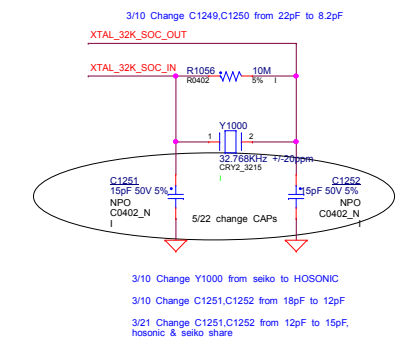
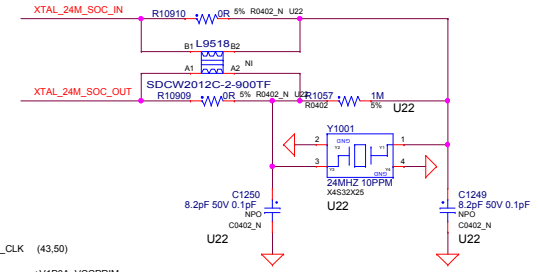
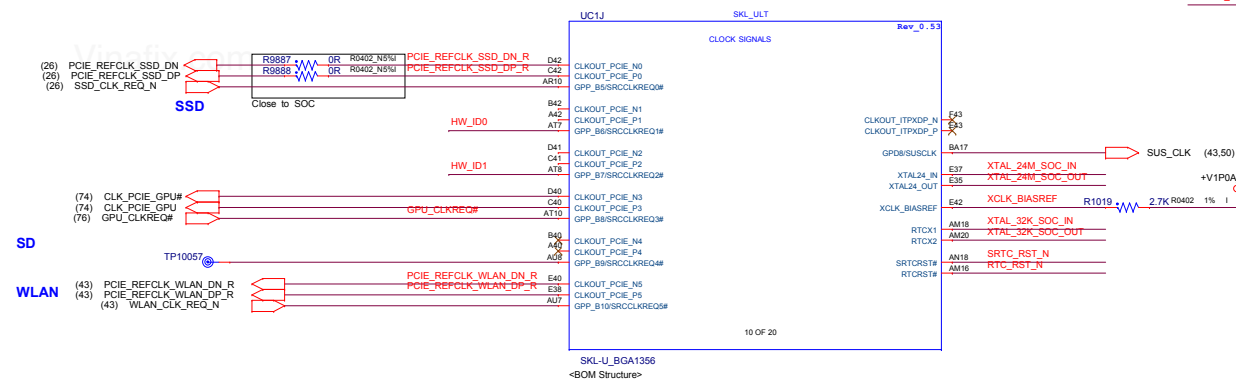
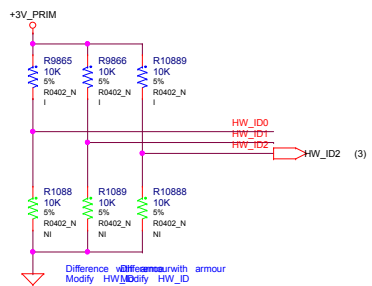


Difference with armour
Add 0ohm NI

5/10 Del TP1055,TP1056,TP1057,TP1058,TP1059,TP1060,TP1016,TP1017,
MIPI differential don't test point



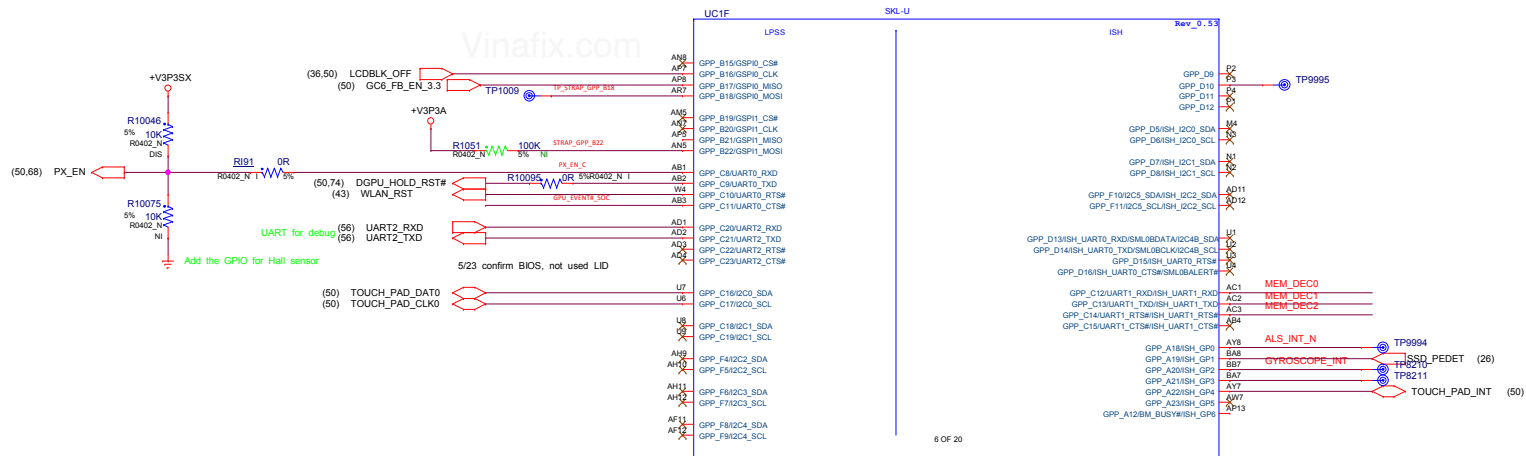
Project: 330S-KBL Series	
Engineer: Luffy	
Size	Title: KBL-U(4/12)HDA,EMMC,SD
Custom	Rev V01
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224 Add R1042,VR_PWRGD connect to SOC and EC

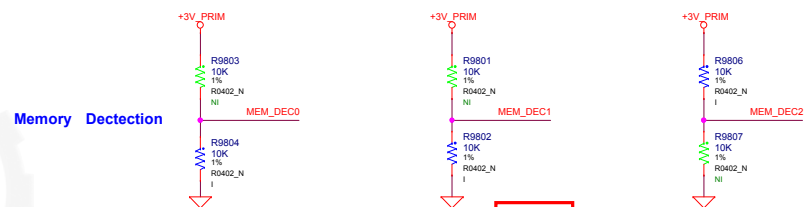
CHG_ACOK change to ACPRES from Charger IC

Project: 330S-KBL Series		Rev: V01	
Engineer: Luffy		Date: Tuesday, September 26, 2017	
Size: Custom	Title: KBL-U(5/12)CLK,GPIO	Sheet: 7	of: 81



- +3V_PRIM
- +V3P3SX
- +V3P3A
- +V3P3SX (5.6,7.9,10,20,25,26,27,28,30,35,36,43,46,50,52)
- +V3P3A (3,4,5,6,7,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)

(76) GPU_EVENT# DIS SOD_323 BAT54WS D6607 GPU_EVENT#_SOC

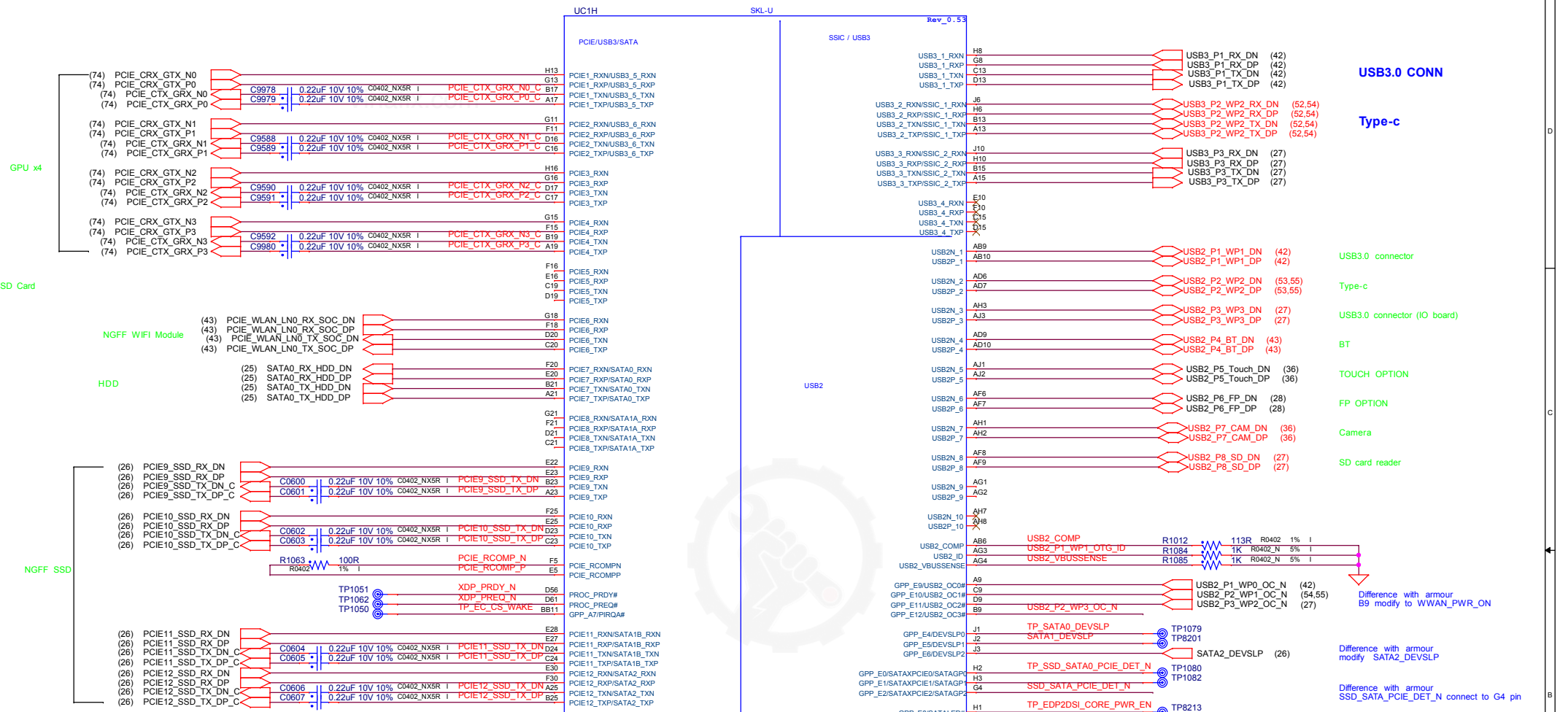


	Samsung_4GB	Micron_4GB	Hynix_4GB	Samsung_8GB	Micron_8GB	Hynix_8GB	Samsung_16GB	Micron_16GB
MEM_DEC0	0	1	0	1	0	1	0	1
MEM_DEC1	0	0	1	1	0	0	1	1
MEM_DEC2	0	0	0	0	1	1	1	1

Default

GSP10_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XPDP. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSP11_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCH, bit 6). Bit 6 Boot BIOS Destination 0 SPI (Default) 1 LPC Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GBE LAN. 4. This signal is in the primary well.

Keyparts	Character	Supplier	Description	3NOD PN	Lenovo P/N
Lenovo B/S part sourcing plan					
CPU	Intel® 6th Gen Core™	Intel	i3-6100U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i3-6100U 2.3G/2C/3M intel)	457100266700	SSA0K07374
		Intel	i5-6200U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i5-6200U 2.3G/2C/3M intel)	457100266800	SSA0K07375
		Intel	i7-6500U 2.5G/2C/4M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i7-6500U 2.5G/2C/4M intel)	457100266900	SSA0K07377
DRAM	4Gbx16 DDR4 2400 SDRAM (单颗容量 0.5GB)	Samsung	K4A4G165WE-BCRC (MEMORY DDR4-2400 256Mx 16 96FBGA K4A4G165WE-BCRC Samsung SM30L08878)	403670650600	SM30L08878
		Micron(Elpida)	MT40A256M16GE-083E.B		SM30L08871
		Hynix	H5AN4G6NAFR-UHC (MEMORY DDR4 2400 256M x 16 96ball FBGA H5AN4G6NAFR-UHC Hynix SM30L08876)	403670650800	SM30L08876
	8Gbx16 DDR4 2400 SDRAM (单颗容量 1GB)	Samsung	K4A8G165WB-BCRC (MEMORY DDR4-2400 512Mx 16 96FBGA K4A8G165WB-BCRC Samsung SM30L08874)	403670650700	SM30L08874
		Micron(Elpida)	MT40A512M16JY-083E.B	403670650900	SM30L08877
		Hynix	H5AN8G6NAFR-UHC (MEMORY DDR4 2400 512M*16 96FBGA MT40A512M16JY-083E.B Micron SM30L08877)		SM30L08875



Difference with armour
SSD interface SATA change to PCIe
SATA1A change to PCIe port 9,10,11,12

Checklist
Gen1 and Gen2=100nF
Gen3=220nF

High Speed I/O (HSIO) Lane Multiplexing in SKL U

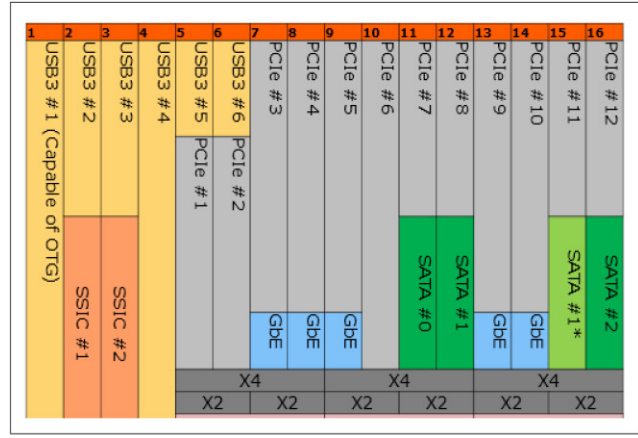
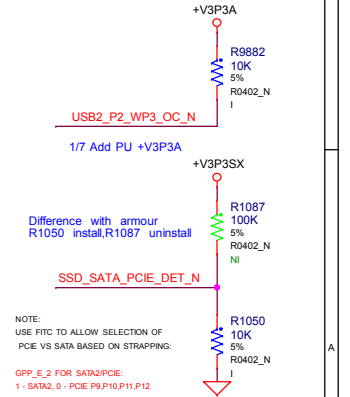


Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	SATA	SATA	PCIe/LAN	PCIe/LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*/ USB 3.0	PCIe*/ USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	PCIe/SATA	PCIe/SATA	PCIe/LAN	PCIe/LAN	PCIe/SATA	PCIe/SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*/ USB 3.0	PCIe*/ USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	PCIe/SATA	PCIe/SATA	PCIe/LAN	PCIe/LAN	N/A	N/A

+V3P3A
+V3P3SX

GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

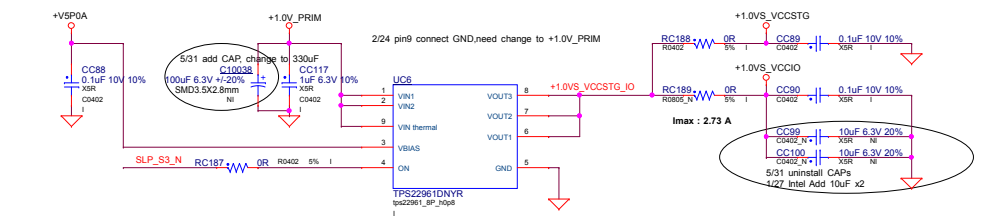
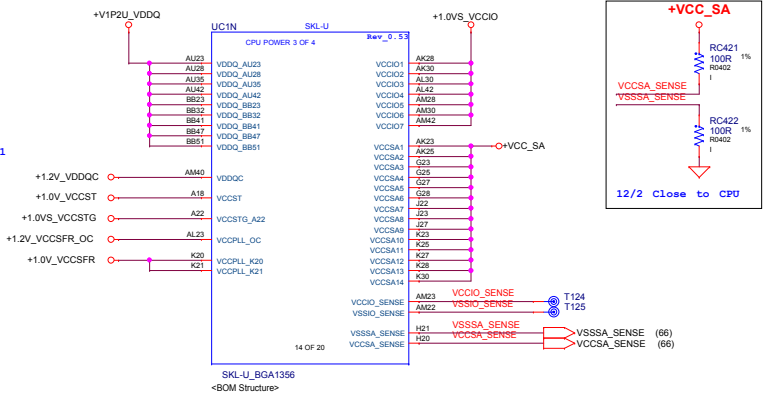
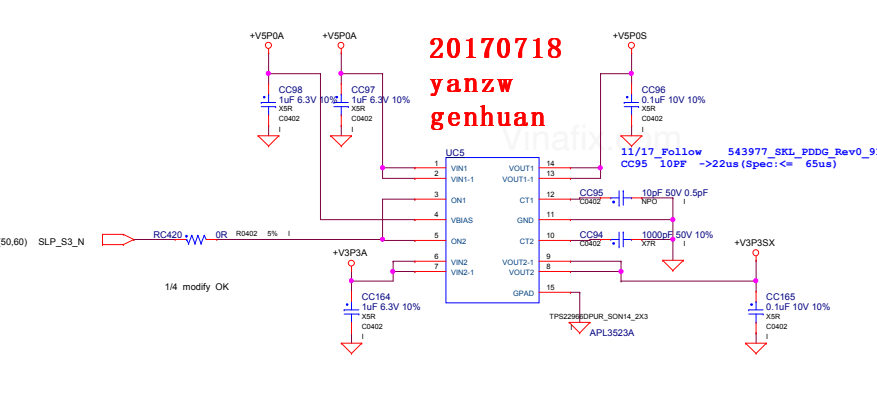


NOTE:
USE FITC TO ALLOW SELECTION OF
PCIe VS SATA BASED ON STRAPPING:
GPP_E3 FOR SATA/PCIe:
1-SATA, 0-PCIe P9:P10:P11:P12

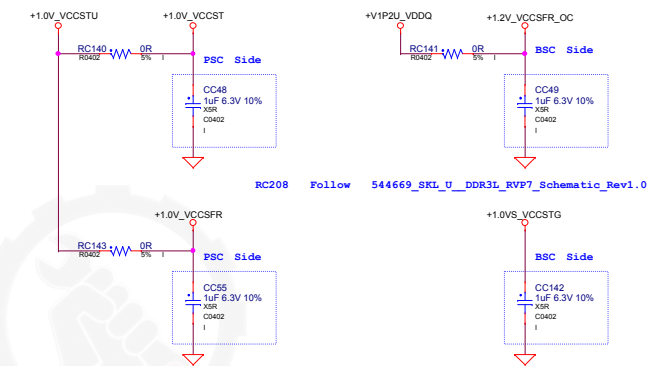
Project: 330S-KBL Series
Engineer: Luffy

Size	Title: KBL-U(7/12)PCIe,USB,SATA	Rev
Custom		V01
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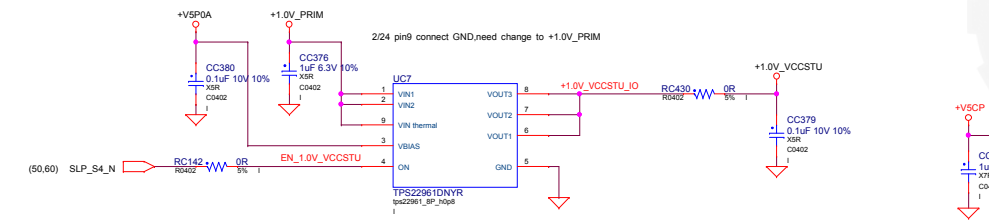
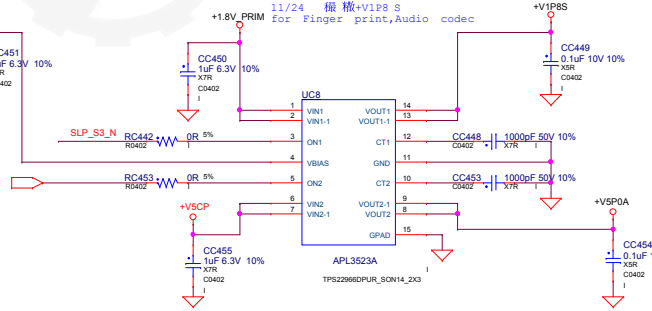
20170718 yanzw genhuan



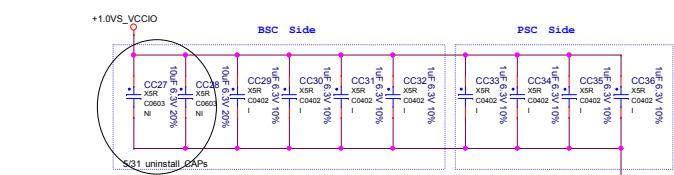
+1.0V_PRIM to +1.0VS_VCCSTG / +1.0VS_VCCIO



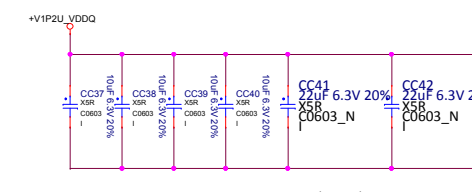
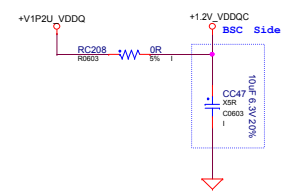
+1.8V_PRIM to +V1P8S



+1.0V_PRIM to +1.0V_VCCSTU



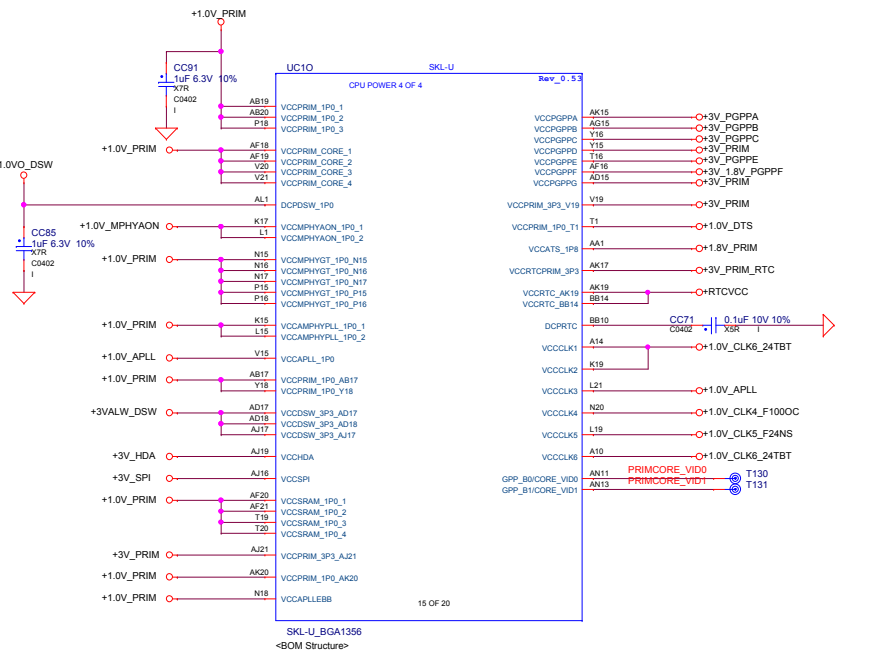
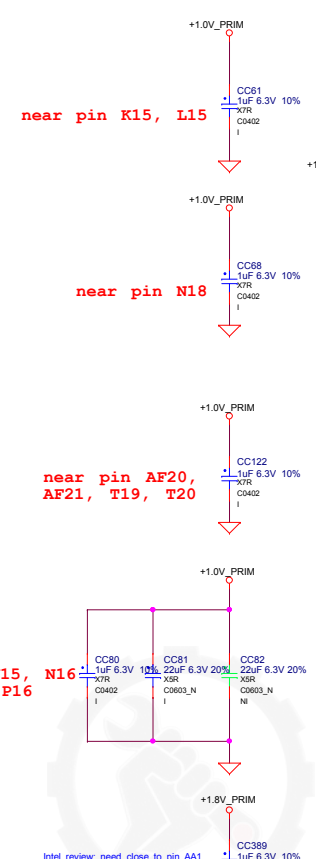
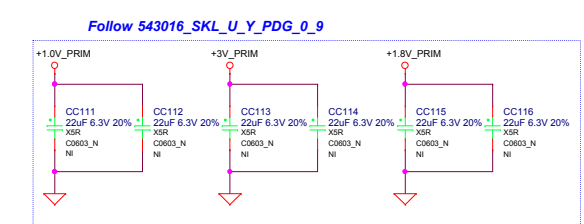
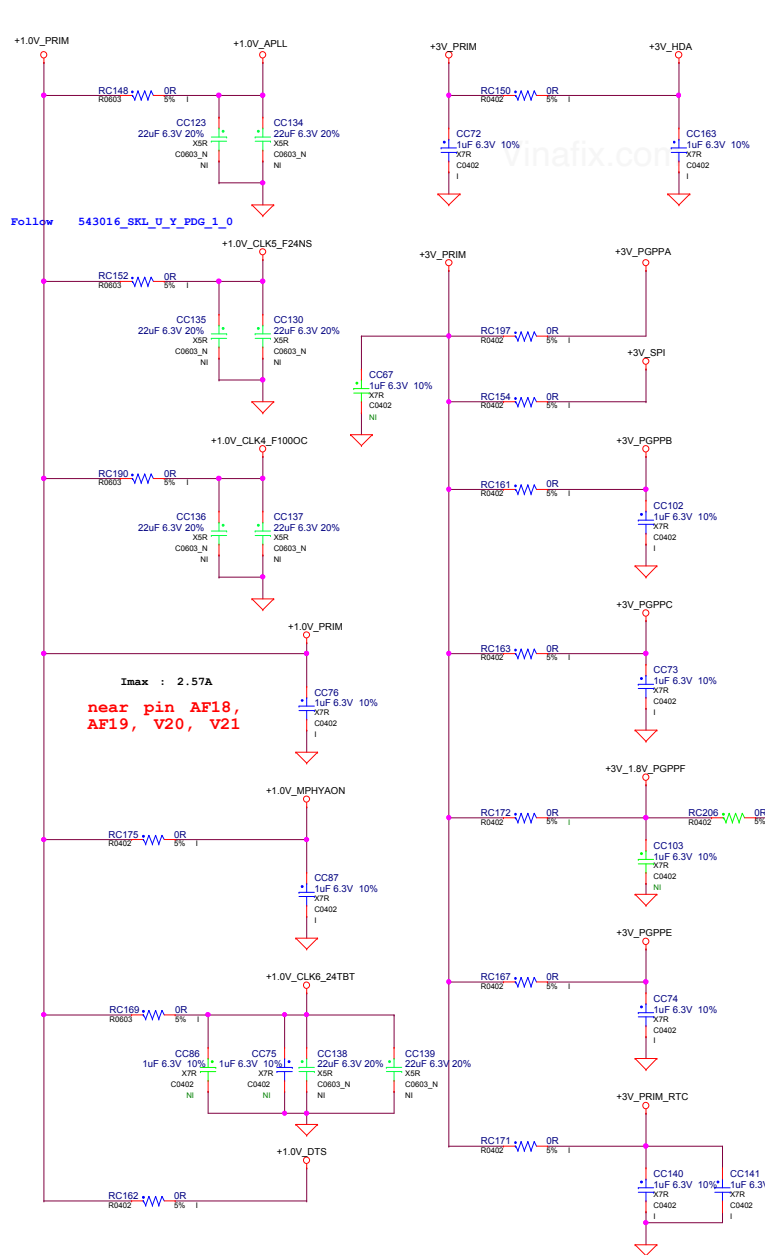
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53



+V1P2U_VDDQ: 10UF/6.3V/0603 *4
22UF/6.3V/0402 *3

- +VCC_SA (15.67)
- +V1P8S (8)
- +VSCP (42.60)
- +1.8V_PRIM (11,45,56,65)
- +V3P8A (5,4,5,6,7,8,5,11,20,24,26,27,29,30,42,50,51,55,56,60,62,65,66,68,69)
- +VSP0S (25,30,35,36,46)
- +VSP0A (11,24,27,50,54,61,62,63,65,66,67,68,69,70,72)
- +1.0V_PRIM (11,14,63)
- +V3P8X (5,6,7,8,9,20,25,26,27,28,30,35,36,43,46,50,52)
- +V1P2U_VDDQ (4,19,20,21,61,68)
- +1.0VS_VCCSTG (3,12)
- +1.0VS_VCCIO (3,14)

Project: 330S-KBL Series		Rev: V01
Engineer: Luffy		Rev: V01
Size: C	Title: KBL-U(8/12)Power	Rev: V01
Date: Tuesday, September 26, 2017	Sheet: 10	of 81

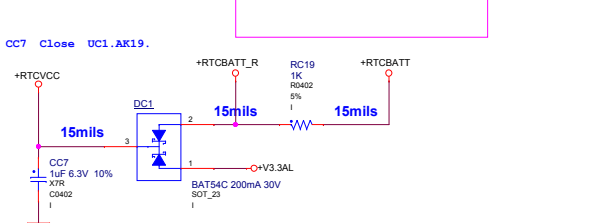


Per 543016_SKL_U_Y_PDG_0_9
VDCRTC does not exceed 3.2 V from PDG

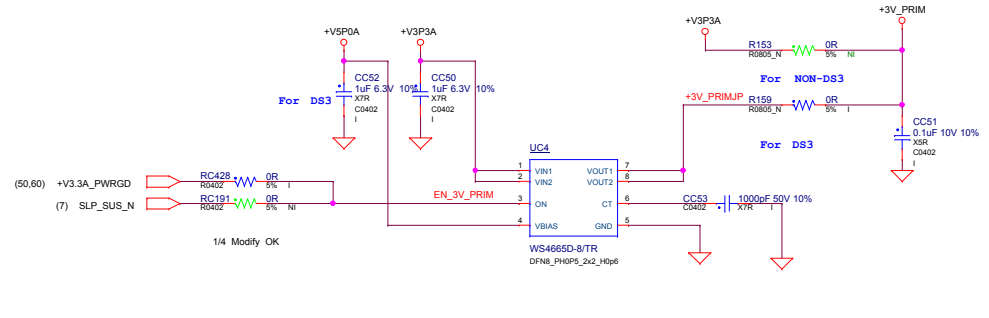
Power Rail	Voltage
+CHGRTC	3.383V (MAX)
BAT54C (VF)	240 mV
+3VL_RTC	3.143V

Result : Pass

RTC Battery

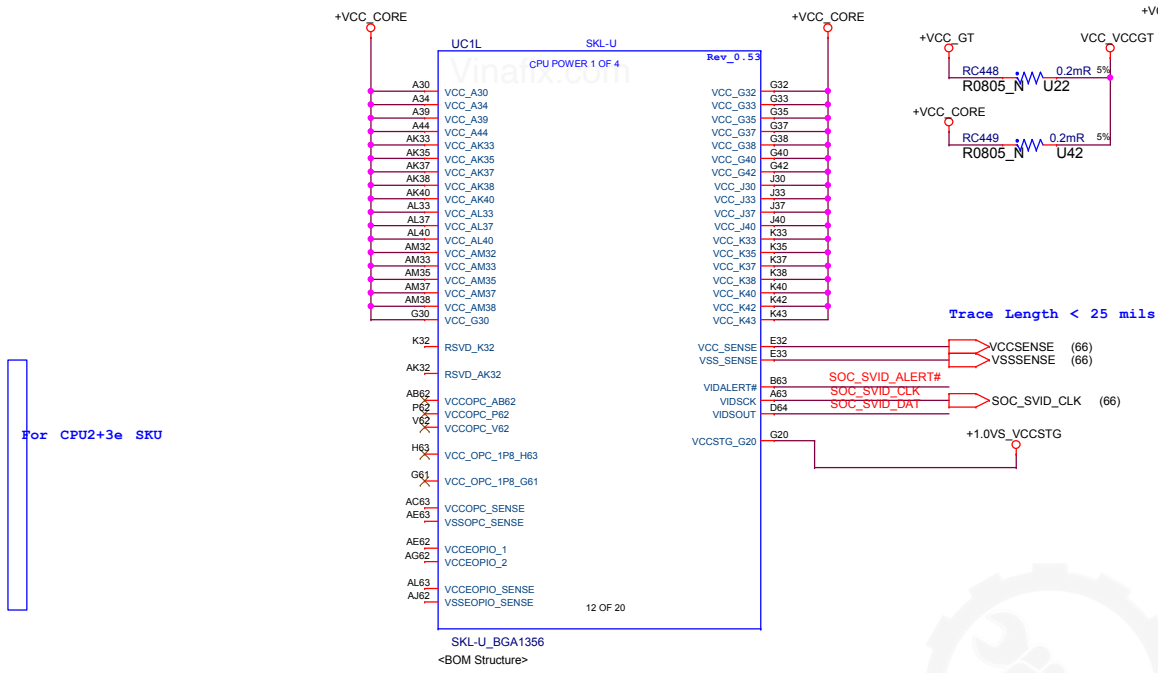


+V3P3A to +3V_PRIM

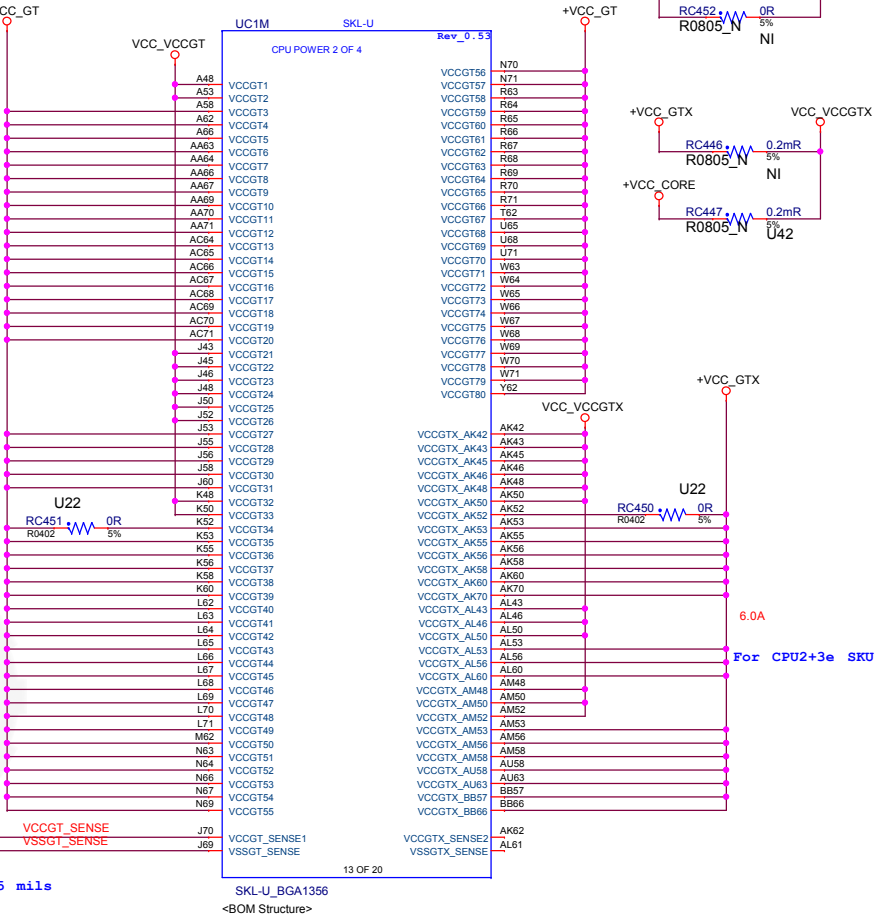


- +RTCVCC (7)
- +1.0V_PRIM (10,14,63)
- +3V_PRIM (7,8)
- +1.8V_PRIM (10,46,56,65)
- +V3P3A (3,4,5,6,7,8,9,10,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)
- +V5P0A (10,24,27,50,54,61,62,63,65,66,67,68,69,70,72)

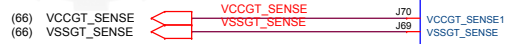
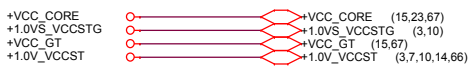
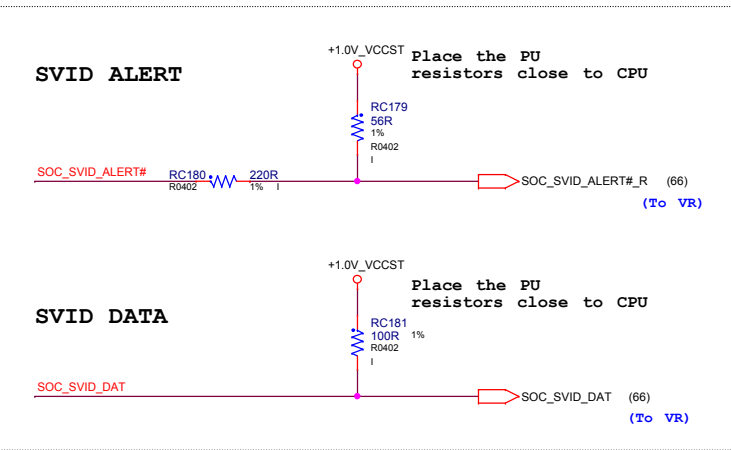
Project: 330S-KBL Series	
Engineer: Luffy	
Size	Title: KBL-U(9/12)Power
Custom	
Date: Tuesday, September 26, 2017	Sheet 11 of 81



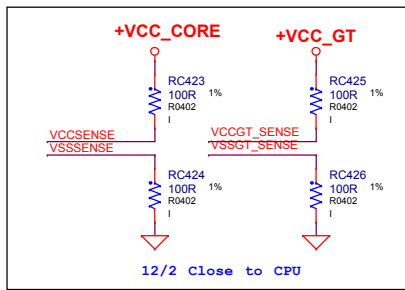
For CPU2+3e SKU



For CPU2+3e SKU



Trace Length < 25 mils



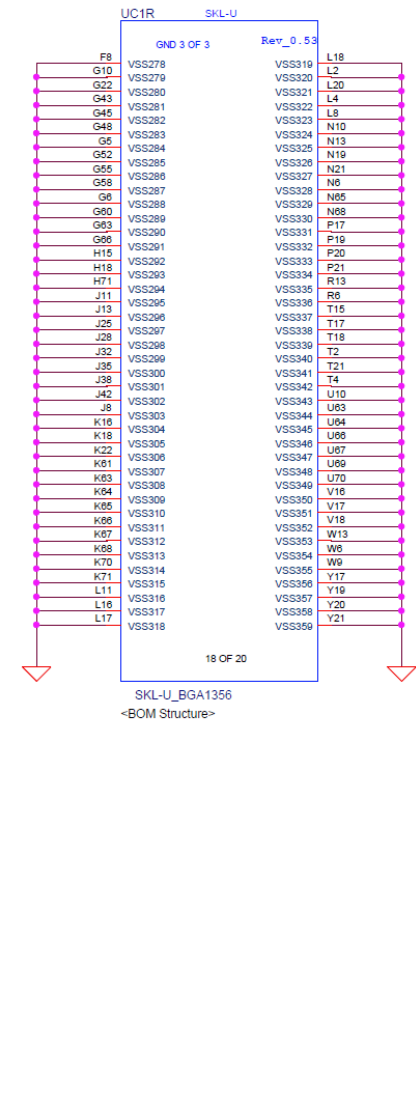
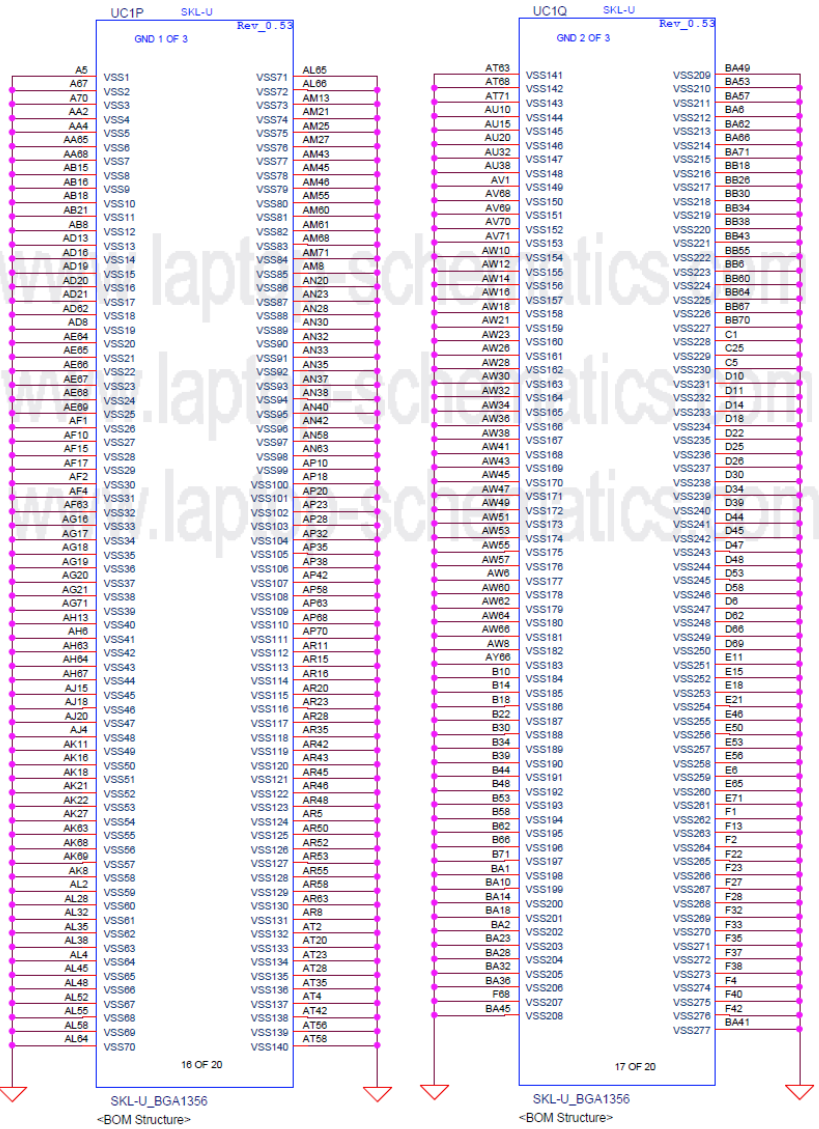
Package Sensing Recommendations

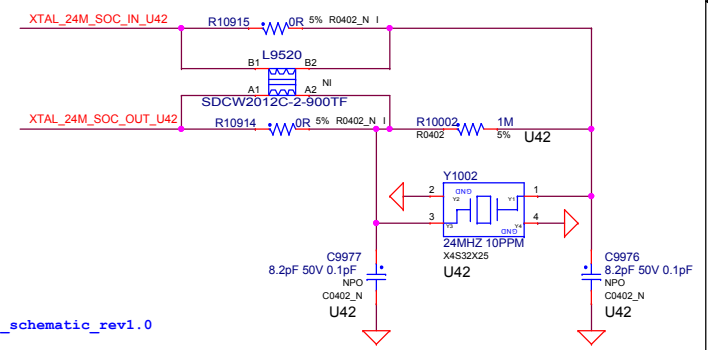
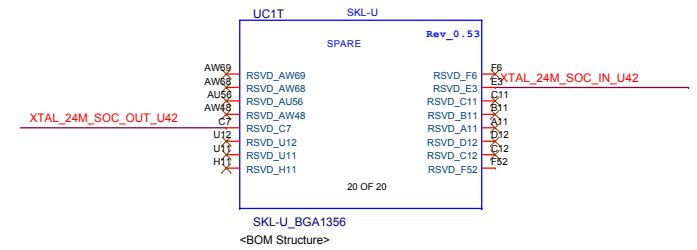
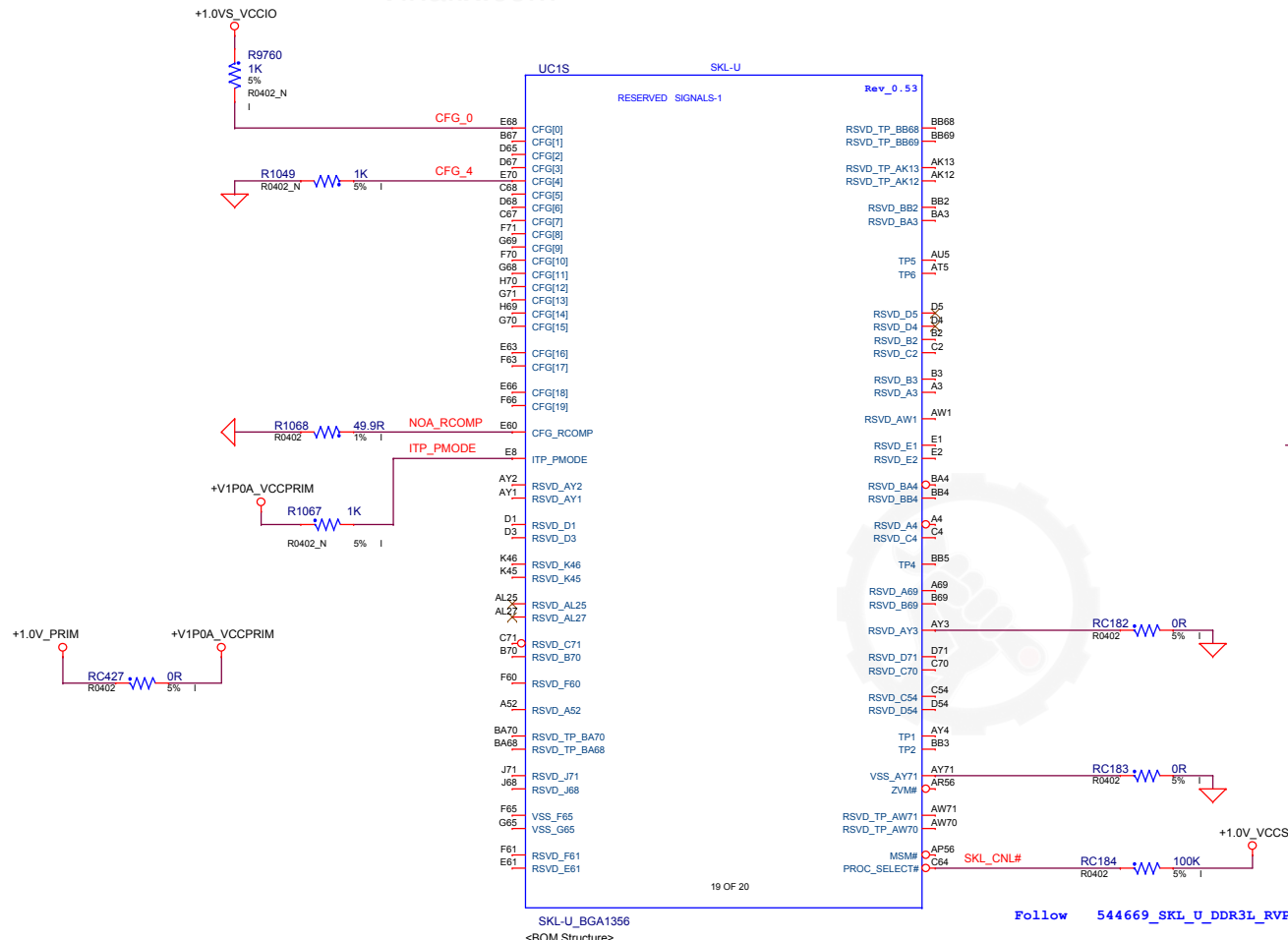
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccsA_SENSE / VssSA_SENSE			
VccIO_SENSE / VssIO_SENSE[1]			
		NA	

Note: [1] Does not apply when rails are merged.

Project: 330S-KBL Series
Engineer: Luffy

Size: Custom Title: **KBL-U(10/12)Power,SVID** Rev: V01
 Date: Tuesday, September 26, 2017 Sheet 12 of 81





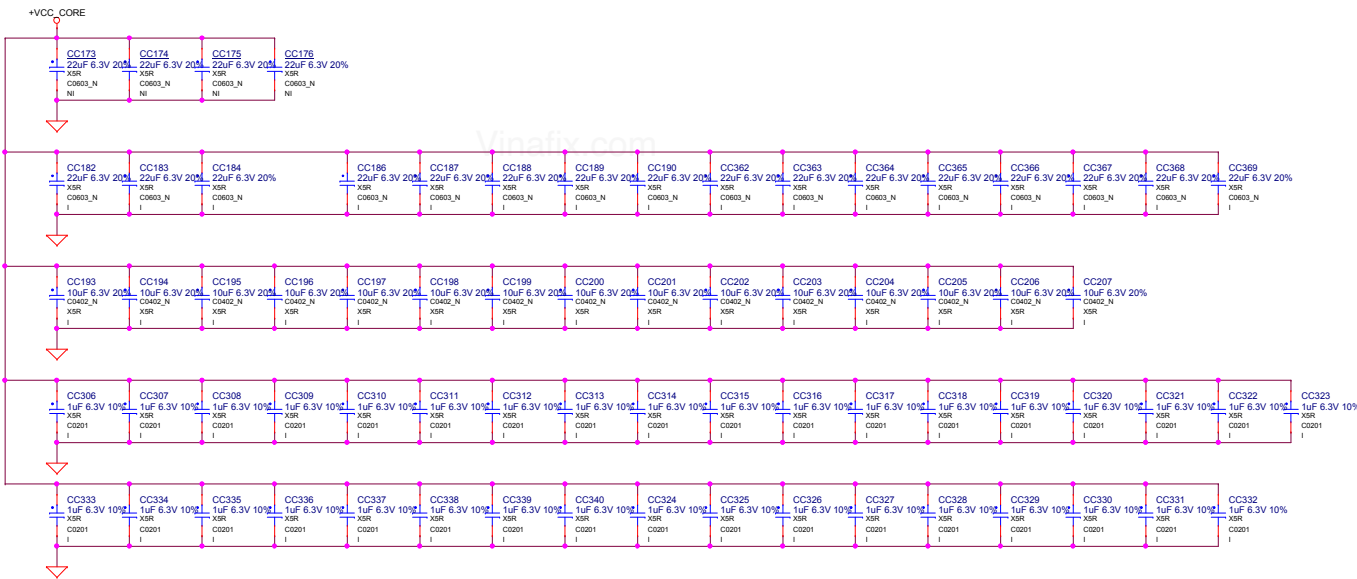
Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

For 2+3e Solution
PM_ZVM#
PM_MSM#

- +1.0VS_VCCIO (3,10)
- +V1P0A_VCCPRIM (7)
- +1.0V_PRIM (10,11,63)
- +1.0V_VCCST (3,7,10,12,66)

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

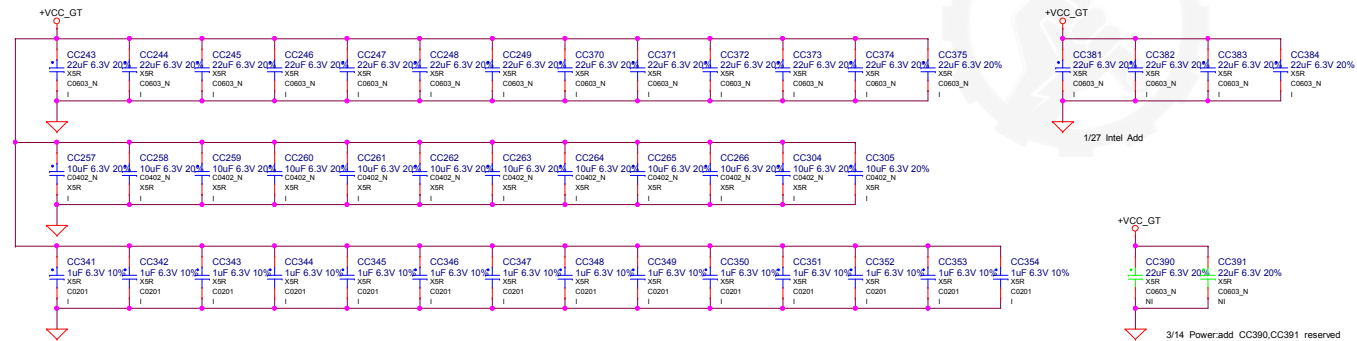
Project: 330S-KBL Series	
Engineer: Luffy	
Size	Title: KBL-U(12/12)RSVD
Rev	V01
Custom	
Date: Tuesday, September 26, 2017	Sheet 14 of 81



12/30 check PDG
& 220uF pull power side

+VCC_CORE

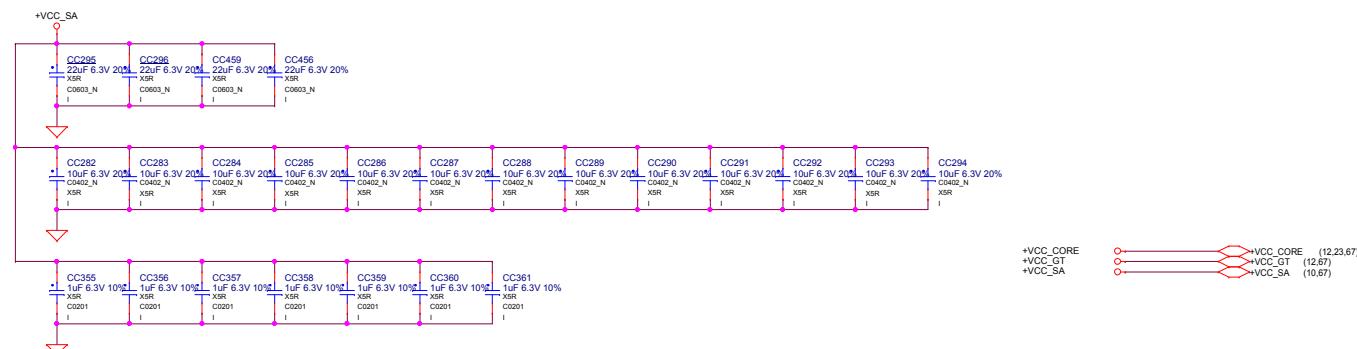
47uF x8 change 47uF x4
 22uF x9 change 22uF x17
 10uF x15
 1uF x35



12/30 check PDG
& 220uF pull power side

+VCC_GT

47uF x3 change 47uF x0
 22uF x7 change 22uF x13
 10uF x12
 1uF x14



+VCC_SA

12/30 check PDG

47uF x2
 10uF x13
 1uF x7



Project: 330S-KBL Series	
Engineer: Luffy	
Size	Title: SOC (DECOUPLING)
Rev	Rev
Date: Wednesday, September 27, 2017	Sheet 15 of 81

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		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
B		V01
Date:	Tuesday, September 26, 2017	Sheet 16 of 81

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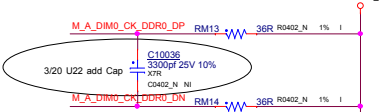
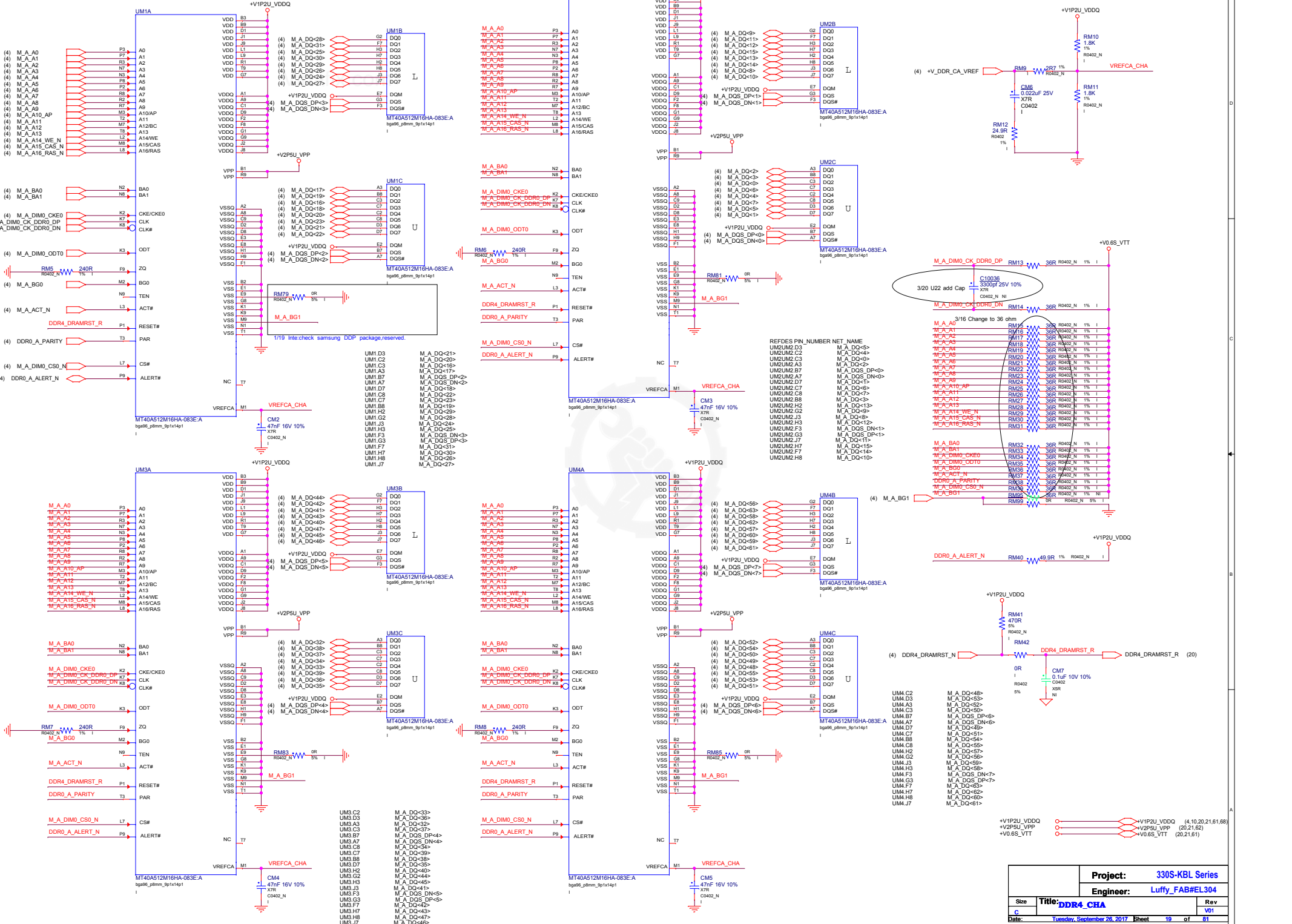


		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
B		V01
Date: Tuesday, September 26, 2017		Sheet 17 of 81

Vinafix.com



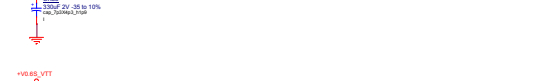
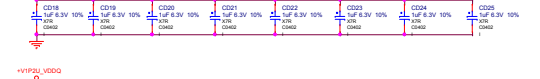
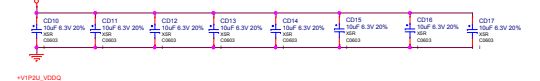
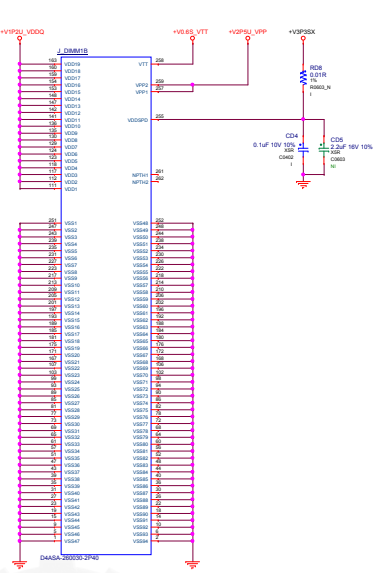
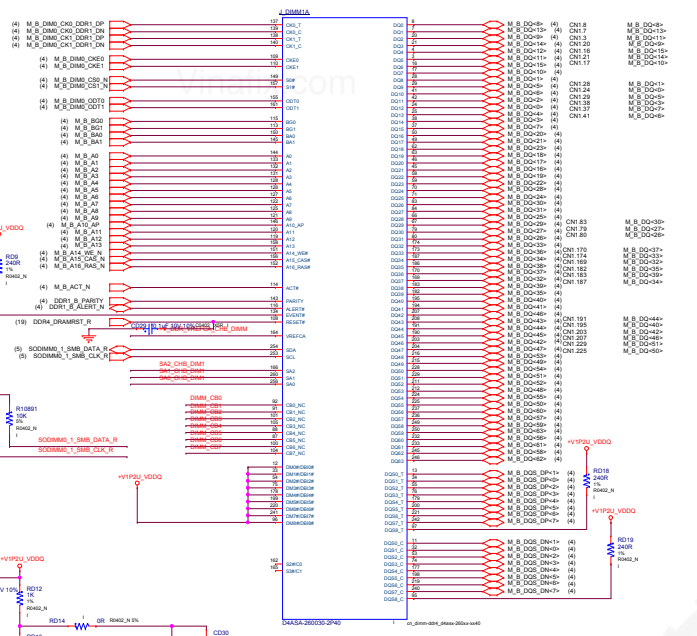
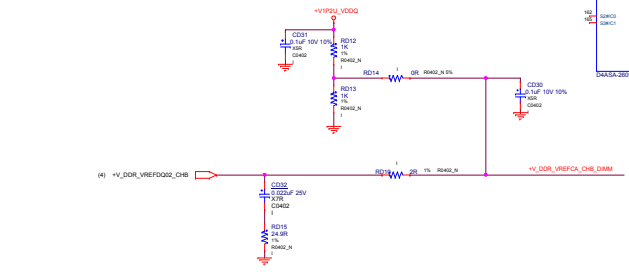
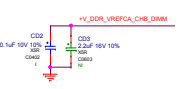
		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date:	Tuesday, September 26, 2017	Sheet 18 of 81



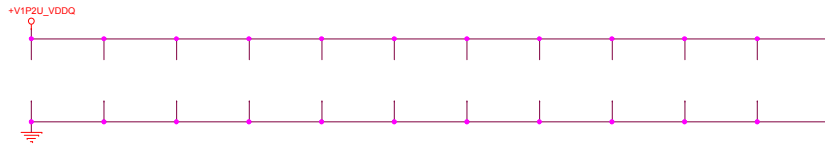
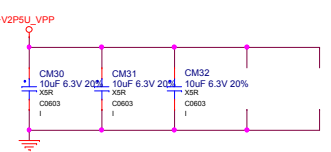
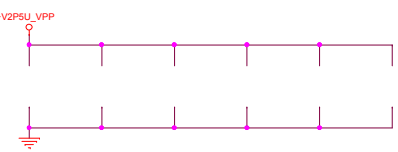
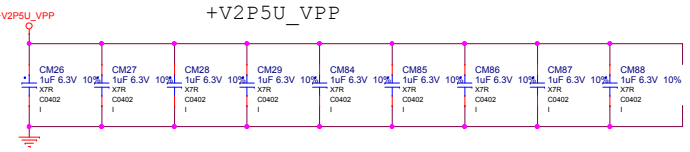
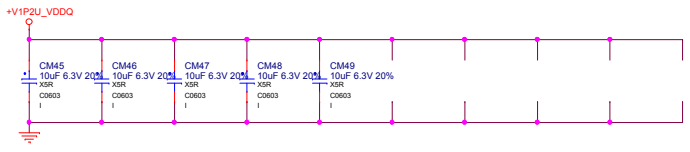
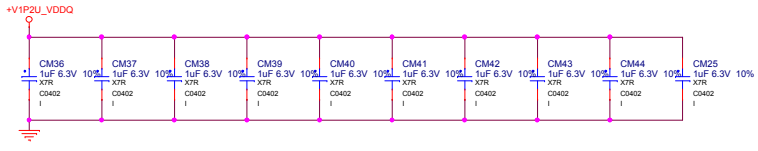
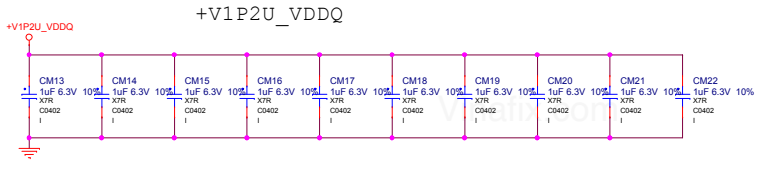
Project: 330S-KBL Series		Rev: V1
Engineer: Luffy_FAB#EL304		Date: Tuesday, September 26, 2017
Size: C	Title: DDR4_CHA	Sheet: 19 of 81

- +VIP2U_VDDQ
- +V2P5U_VPP
- +V0.6S_VTT
- +VIP2U_VDDQ (4.10.20.21.61.68)
- +V2P5U_VPP (20.21.62)
- +V0.6S_VTT (20.21.61)

CHANNEL-1:
SA0:0
SA1:1
SA2:0



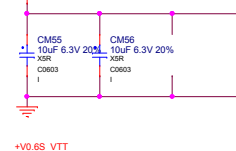
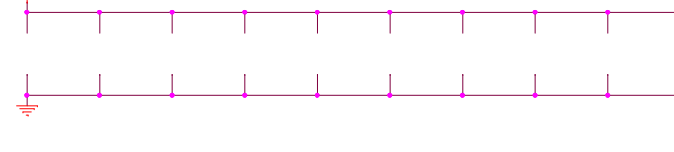
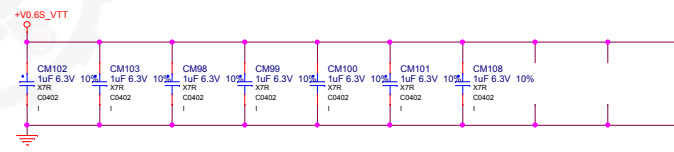
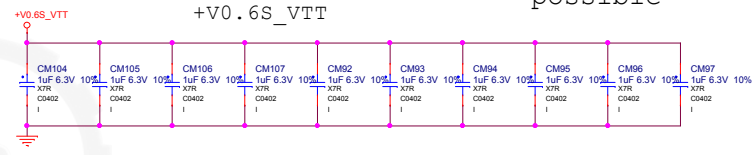
Project:		330S-KBL Series
Engineer:		Luffy (FABWVP204)
Size:	Title:	DDMM_DMMB
Rev:	Ver:	1
Date:	Created:	2017-08-20



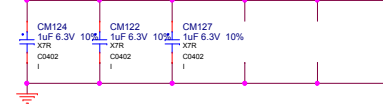
1uF:4 as near each x16
DRAM device as
possible

10uF:Distributed around
the DRAM devices

1uF:2 as near each x20
DRAM device as
possible



10uF:Distributed around
the DRAM devices



3/31 add CAPs

+V1P2U_VDDQ (4.10,19,20,61,68)
+V2P5U_VPP (19,20,62)
+V0.6S_VTT (19,20,61)

Project: 330S-KBL Series	
Engineer: Luffy	
Size: C	Title: DDR4 Decoupling
Date: Tuesday, September 26, 2017	Sheet 21 of 81
Rev: V01	

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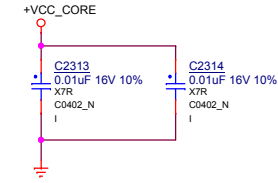


		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date: Tuesday, September 26, 2017		Sheet 22 of 81

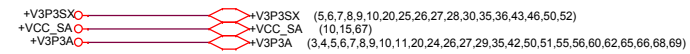
RF Solution

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Cross Moat Cap.

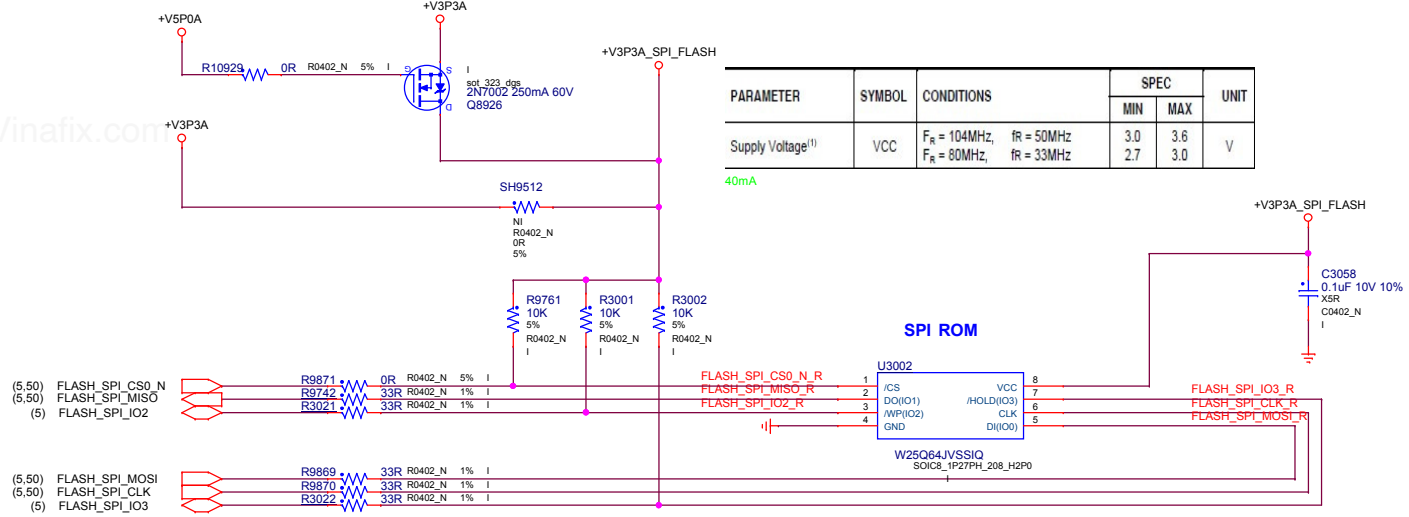


EMC Solution



		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: RF / EMC Solution	Rev
Custom		V01
Date: Tuesday, September 26, 2017	Sheet 23 of 81	

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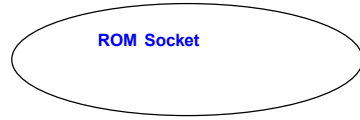


PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage ⁽¹⁾	VCC	F _r = 104MHz, F _r = 80MHz	3.0	3.6	V
		f _r = 50MHz, f _r = 33MHz	2.7	3.0	

- (5,50) FLASH_SPI_CS0_N
- (5,50) FLASH_SPI_MISO
- (5) FLASH_SPI_IO2
- (5,50) FLASH_SPI_MOSI
- (5,50) FLASH_SPI_CLK
- (5) FLASH_SPI_IO3

Difference with ARMOUR
Series-resistor OR
change to 33R

4/5 Remove BIOS Socket



2/24 SIV:Delet ROM Socket @U3002

+V3P3A (3,4,5,6,7,8,9,10,11,20,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)



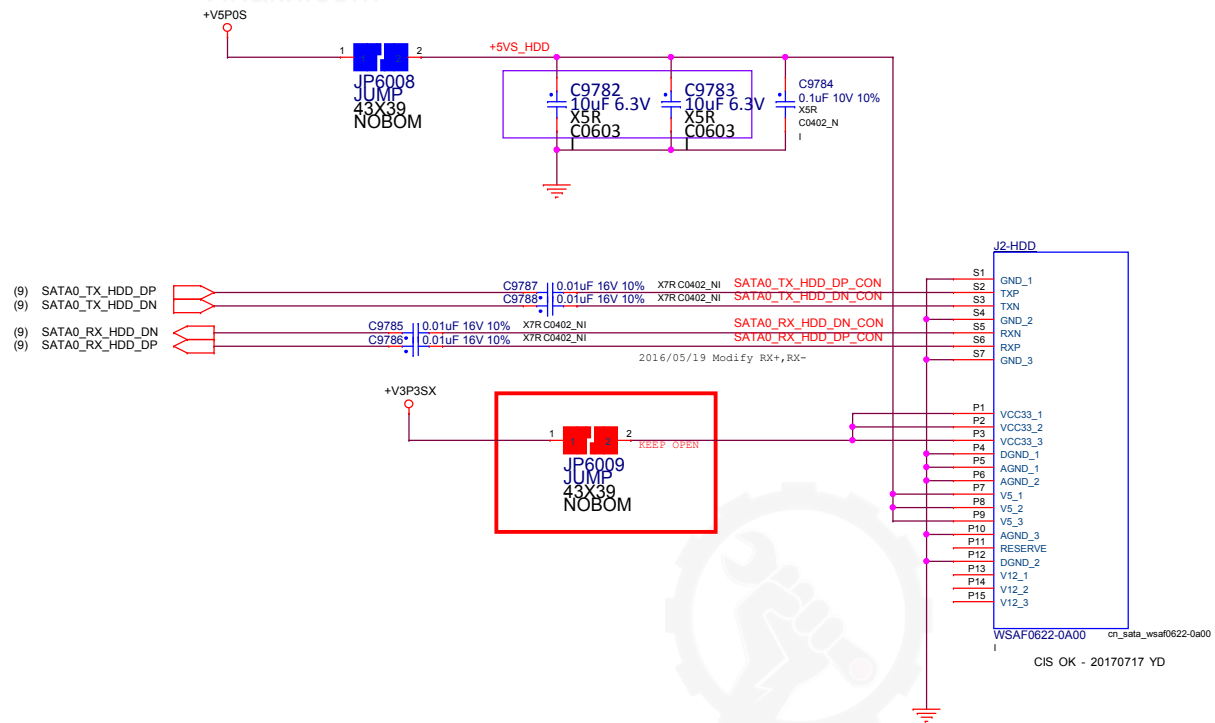
INTERNAL ONLY

BPAGE DRAWING

sky_y_mid.GND
Wed Jun 03 11:22:52 2015

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: SYSTEM FLASH
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 24	of 81

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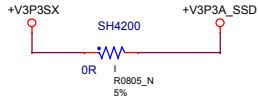
INTERNAL ONLY

BPAGE DRAWING

sky_j_mrd.GND
Wed Jun 03 11:22:52 2015

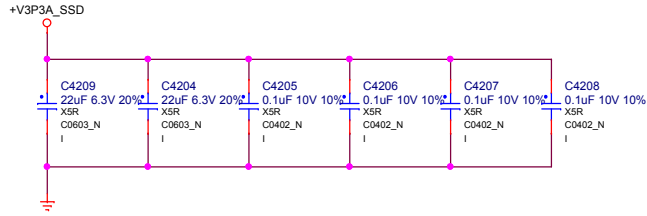
Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title:	HDD	
Custom		Rev V01	
Date:	Tuesday, September 26, 2017	Sheet	25 of 81

M.2 SSD Module
1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD



Change SH4200 0805 shunt to resistor

Vinafix.com



PCIE12 RX
follow intel CRB

Difference with armour
SSD interface SATA change to PCIE
If install SATA CARD,R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF

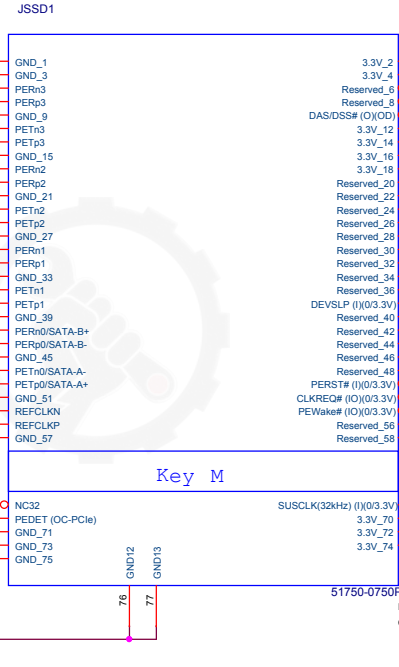
NGFF SSD module interface	PCIE	SATA
Reference	R4200,R4201 install 0ohm C0606,C0607 install 0.22uF	R4200,R4201 install 0.01uF C0606,C0607 install 0.01uF
Detect pin	R1050 install 10Kohm R1087 uninstal 100Kohm	R1050 uninstal 10Kohm R1087 install 100Kohm

Default

3/16 Add SSD(PCIE or SATA) BOM option table

Co-lay PCIE12 RX, reserved R4202,R4203
please close to R4200,R4201

+V3P3SX ○ +V3P3SX (5,6,7,8,9,10,20,25,27,28,30,35,36,43,46,50,52)

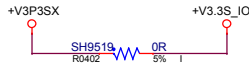


INTERNAL ONLY

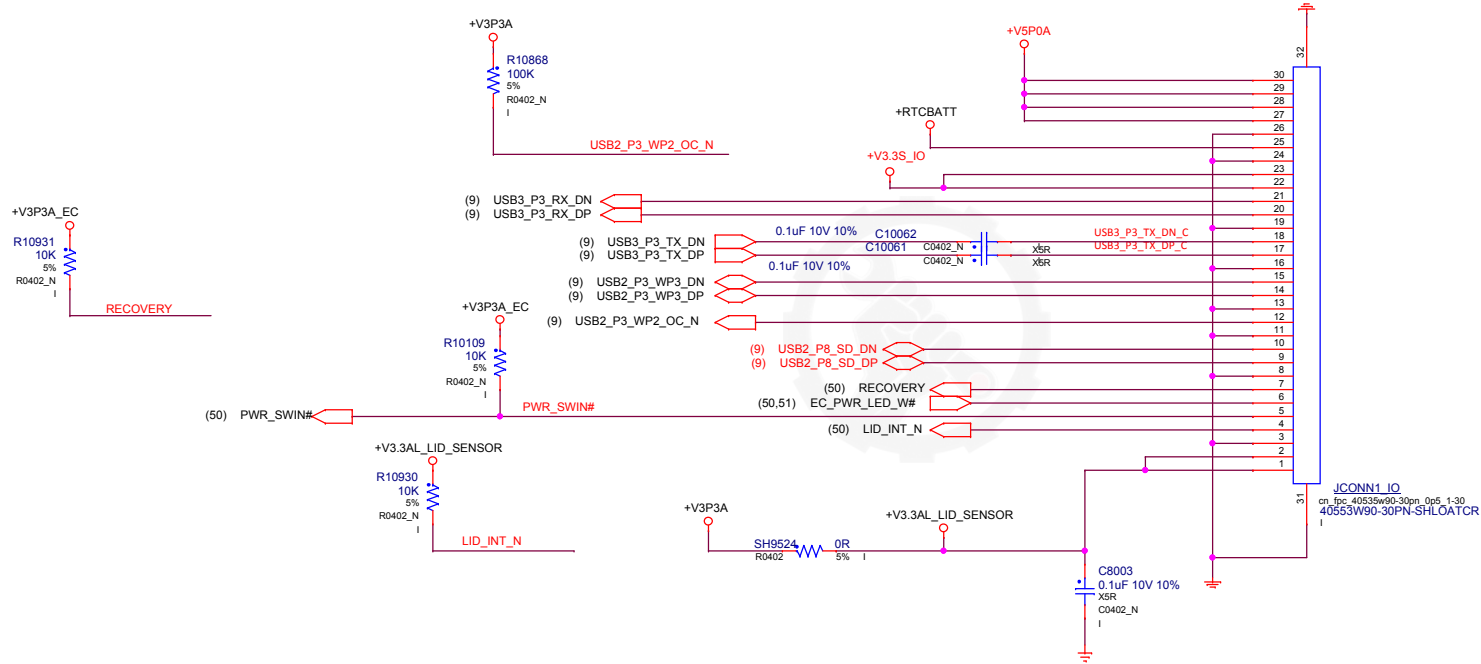
BPAGE DRAWING

shy_x_mrd +V3P3.2k
Wed Jun 03 11:22:52 2015

Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title:	Rev	
Custom	PCIE SSD MODULE	V01	
Date:	Tuesday, September 26, 2017	Sheet	26 of 81



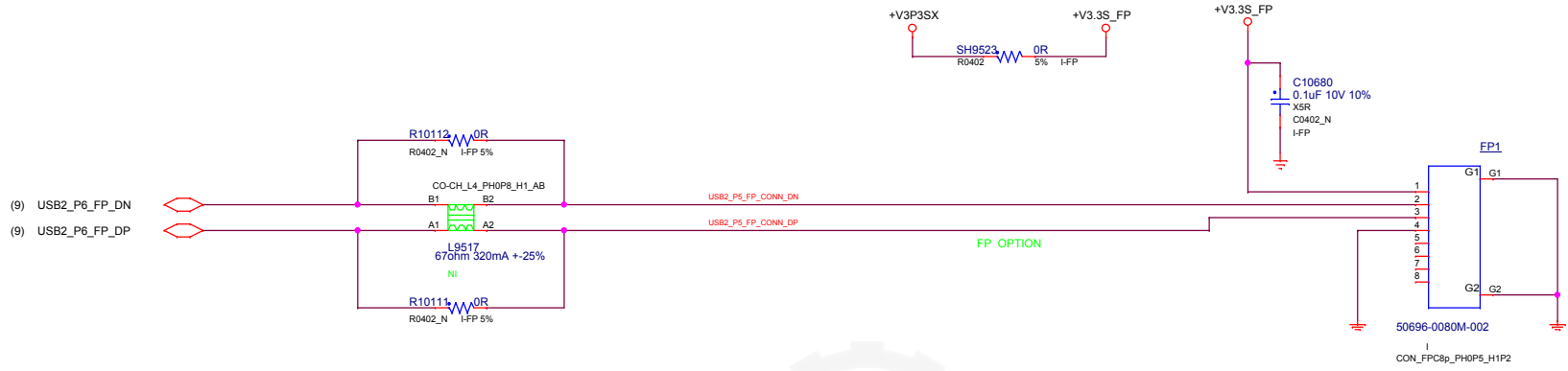
Vinafix.com



JCONN1_IO
 on: fpc_40535w90-30pn_op5_1-30
 40553W90-30PN-SHLOATCR

Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title: IO CONNECTOR	Rev	
Custom		V01	
Date:	Tuesday, September 26, 2017	Sheet	27 of 81

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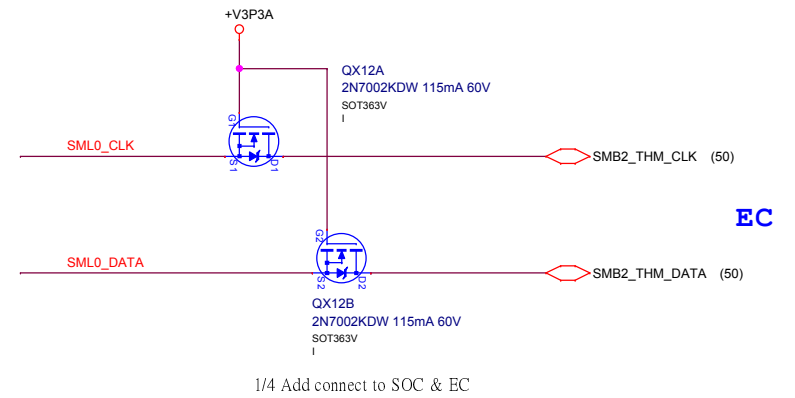
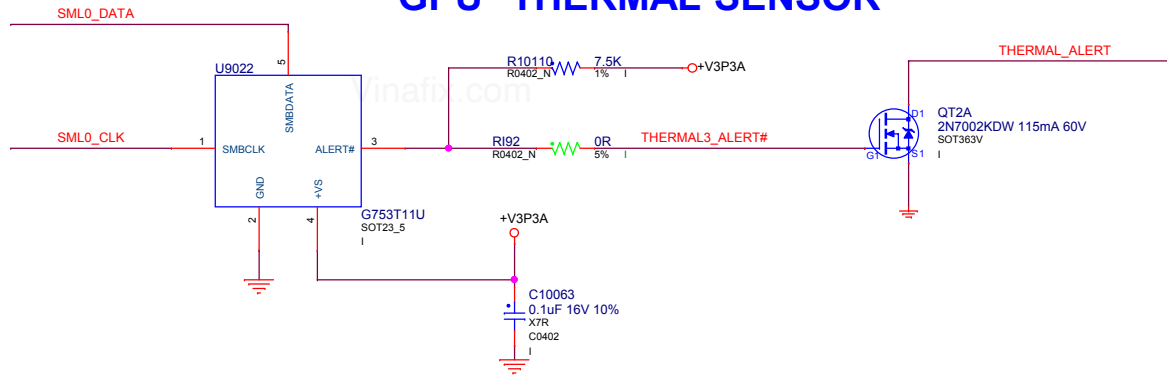
INTERNAL ONLY

BPAGE DRAWING

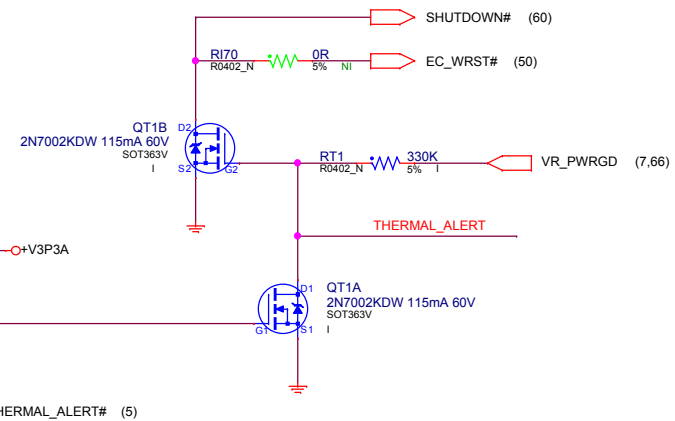
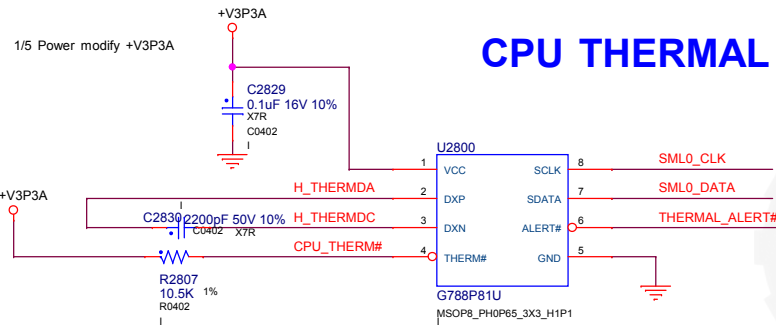
sky_y_mrd: GND
Wed Jun 03 11:22:53 2015

		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: FINGER PRINT		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	28 of 81

GPU THERMAL SENSOR



CPU THERMAL SENSOR



CHARGE THERMAL SENSOR

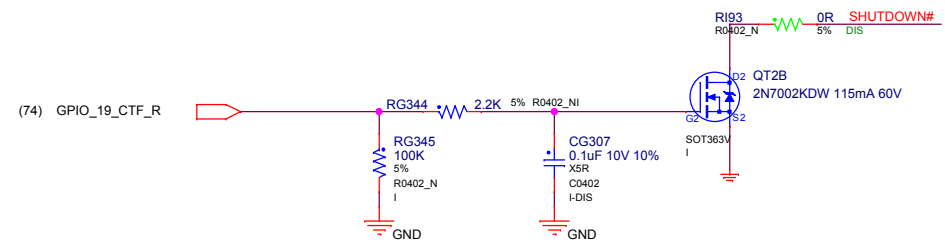
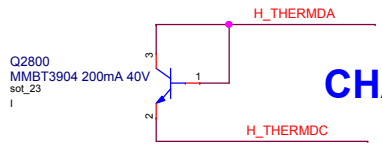


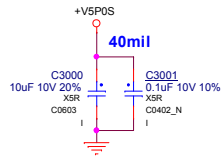
Table 10. Remote temperature THERM limit

The default value is trapping after power up 100ms by different pull-up resistors of THERM and ALERT pin:

TEMPERATURE (°C)		THERM					
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117	
	7.5KΩ	79	89	99	109	119	
	10.5KΩ	81	91	101	111	121	
	14KΩ	83	93	103	113	123	
	18.7KΩ	85	95	105	115	125	

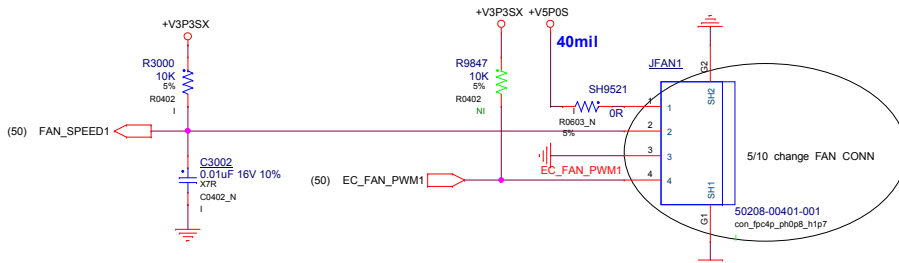
+V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,35,42,50,51,55,56,60,62,65,66,68,69)

Project: 330S-KBL Series	
Engineer: Luffy	
Size	Title: CPU THERMAL SENSOR
Rev	V01
Date: Tuesday, September 26, 2017	Sheet 29 of 81



Vinafix.com

3/7 R9847 connect to +V5P0S,change to +V3P3SX



FAN conn

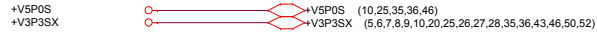
6/21 JFAN1 footprint CON_FPC4P_PH0P6_H1P55 change to con_wb_4p_ph0p6_h1p55_50376

CIS ok

1/11 Update FAN pin define



1. Power Supply (+)
2. FG or RD Output
3. Power Return (-)
4. PWM Input



		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: FAN conn	Rev	
Custom		V01	
Date:	Tuesday, September 26, 2017	Sheet	30 of 81

Vinafix.com



Vinafix.com



INTERNAL ONLY

BPAGE DRAWING

sky_y_red+V3P3.32
Wed Jun 03 11:22:55 2015

		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: NA		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	32 of 81

Vinafix.com



INTERNAL ONLY

BPAGE DRAWING

sky_x_mtd-VIP0.33
Wed Jun 03 11:22:55 2015

		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date: Tuesday, September 26, 2017	Sheet 33	of 81

8

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D

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C

B

B

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A

Vinafix.com



		Project:	330S-KBL Series
		Engineer:	Luffy
Size	Title: NA		Rev
Custom			V01
Date:		Tuesday, September 26, 2017	Sheet 34 of 81

D

D

C

C

B

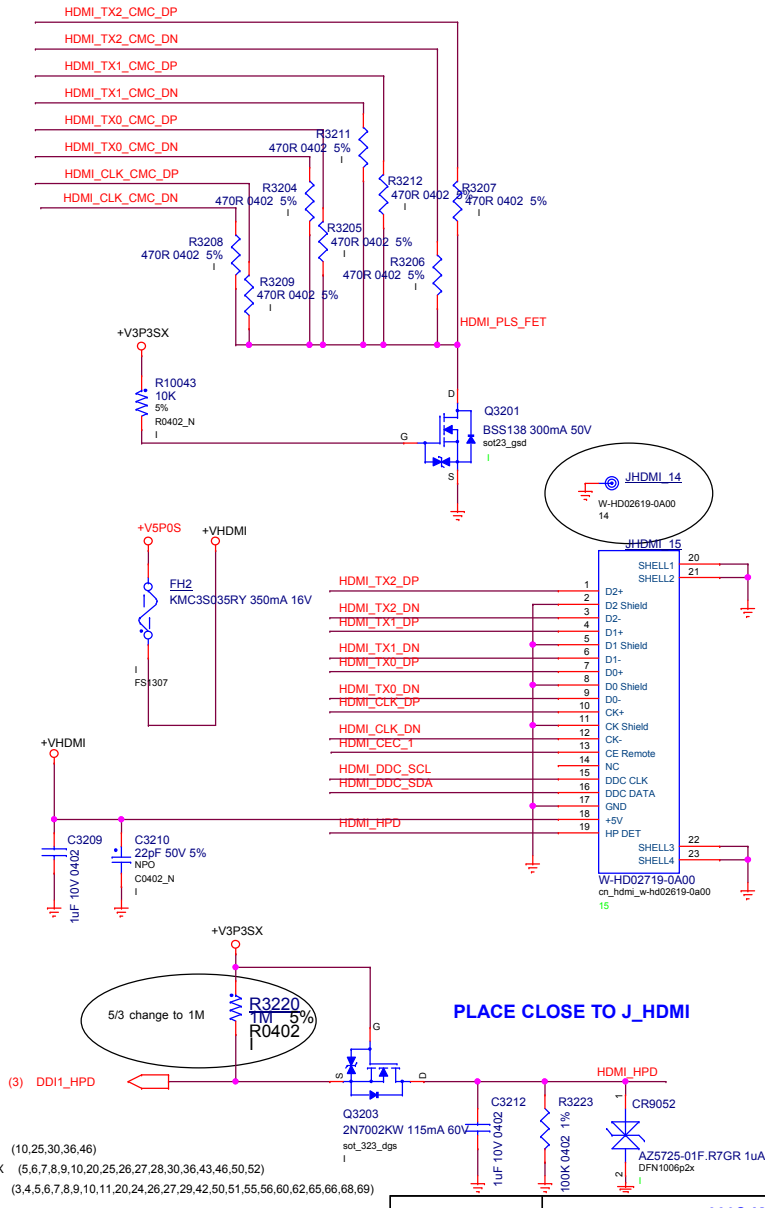
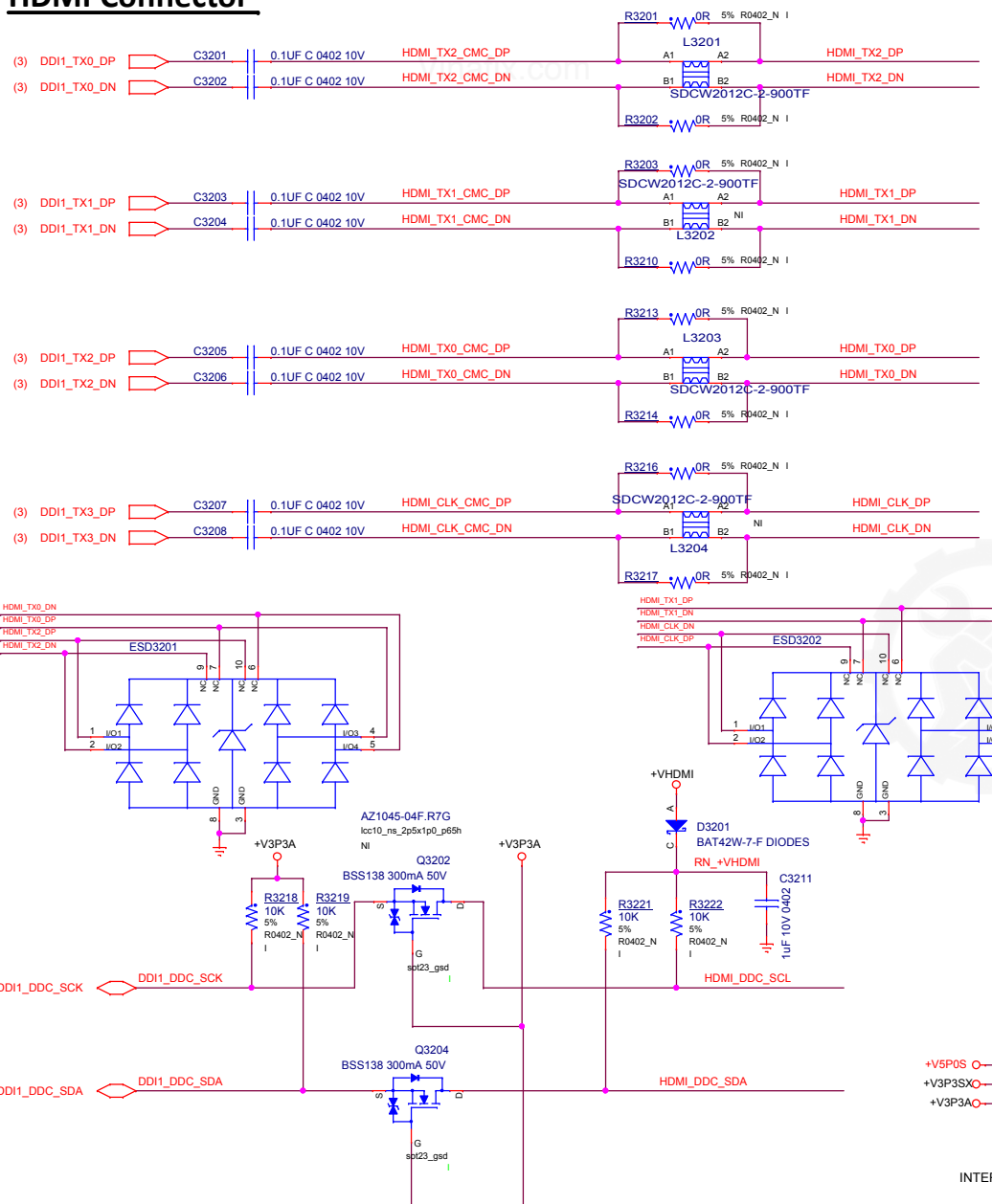
B

A

A

HDMI Connector

for EMI Co-lay



INTERNAL ONLY BPAGE DRAWING

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: HDMI CONNECTOR
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 35	of 81

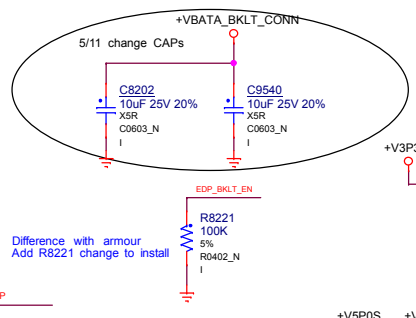
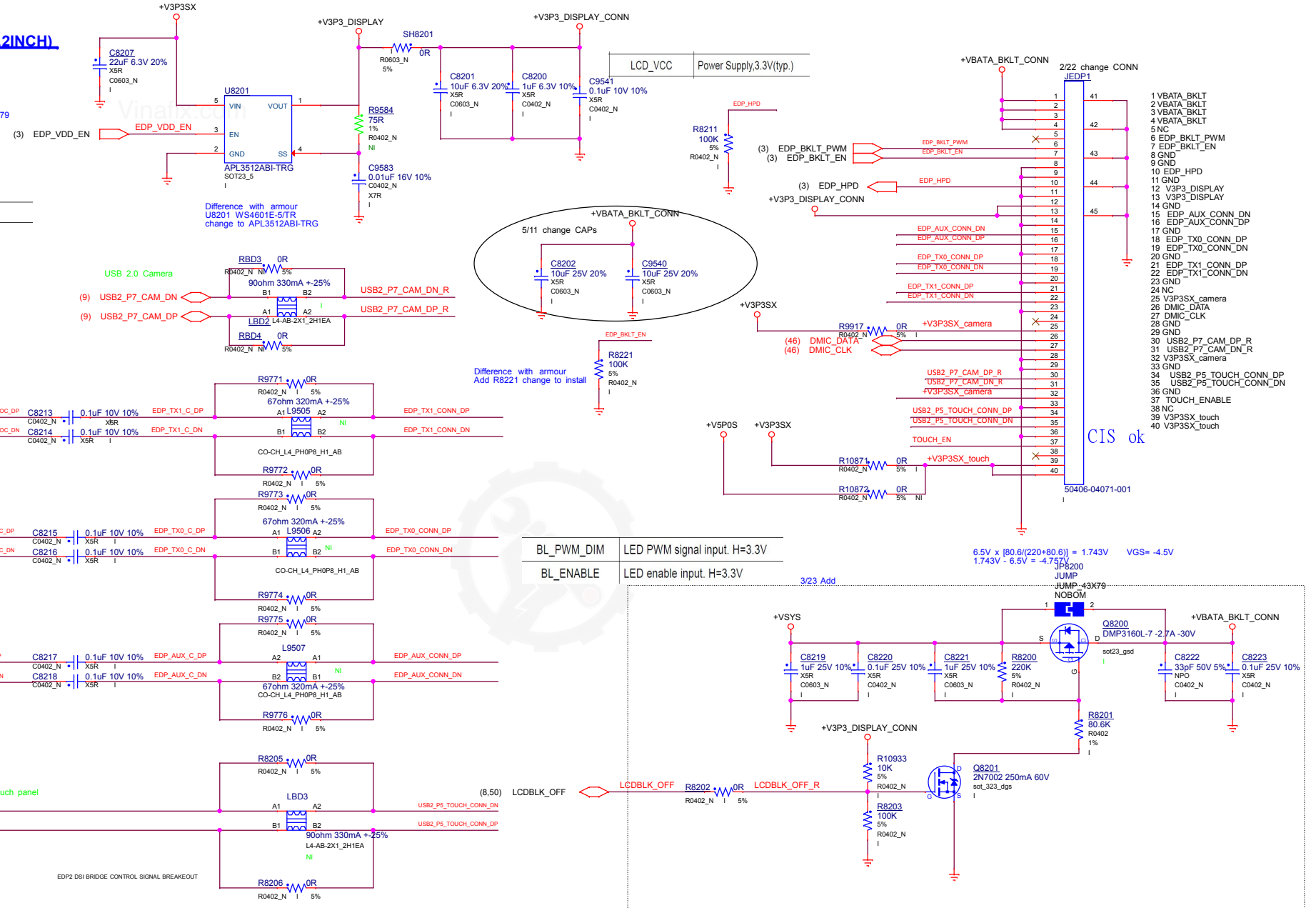
EDP DISPLAY 1920X1200 (12.2INCH)

3/22 FB8200 0603 Bead change to JP8200 JUMP_43X79

BL_PWR | LED Power Supply 6V-8.4V

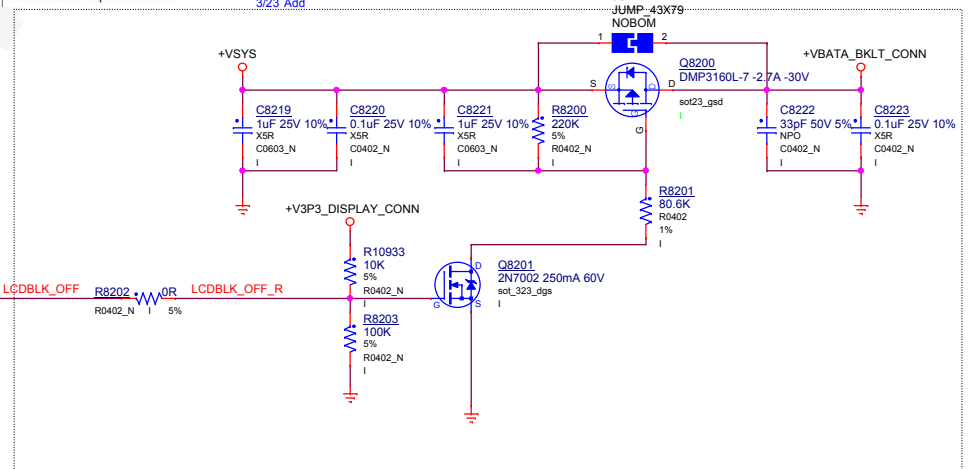
Change the SH8201 0402 shunt to resistor

10	Backlight power consumption	3.94W
11	Panel power consumption	1.03W



BL_PWM_DIM	LED PWM signal input. H=3.3V
BL_ENABLE	LED enable input. H=3.3V

$7.65 \times [80.6 / (220 + 80.6)] = 1.743V$
 $1.743V - 6.5V = -4.757V$
 $6.5V \times [80.6 / (220 + 80.6)] = 1.743V$
 $1.743V - 6.5V = -4.757V$



- 1 VBATA_BKLT
- 2 VBATA_BKLT
- 3 VBATA_BKLT
- 4 VBATA_BKLT
- 5 NC
- 6 EDP_BKLT_PWM
- 7 EDP_BKLT_EN
- 8 GND
- 9 GND
- 10 EDP_HPDP
- 11 GND
- 12 V3P3_DISPLAY
- 13 V3P3_DISPLAY
- 14 GND
- 15 EDP_AUX_CONN_DN
- 16 EDP_AUX_CONN_DP
- 17 GND
- 18 EDP_TX0_CONN_DP
- 19 EDP_TX0_CONN_DN
- 20 GND
- 21 EDP_TX1_CONN_DP
- 22 EDP_TX1_CONN_DN
- 23 GND
- 24 NC
- 25 V3P3SX_camera
- 26 DMIC_DATA
- 27 DMIC_CLK
- 28 GND
- 29 GND
- 30 USB2_P7_CAM_DP_R
- 31 USB2_P7_CAM_DN_R
- 32 V3P3SX_camera
- 33 GND
- 34 USB2_P5_TOUCH_CONN_DP
- 35 USB2_P5_TOUCH_CONN_DN
- 36 GND
- 37 TOUCH_ENABLE
- 38 NC
- 39 V3P3SX_touch
- 40 V3P3SX_touch

CIS ok

50406-04071-001

+V5POS
 +V3P3SX
 +V3P3SX (5,6,7,8,9,10,20,25,26,27,28,30,35,43,46,50,52)

Project:		330S-KBL Series
Engineer:		Luffy
Size	Title:	DISPLAY
Custom		Rev
Date:	Tuesday, September 26, 2017	Sheet 36 of 81

Vinafix.com



BPAGE DRAWING

apl_01.GND
Fri May 27 08:47:32 2016

		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: USB2.0	Rev
Custom		V01
Date:	Tuesday, September 26, 2017	Sheet 37 of 81

D
C
B
A

D
C
B
A

Sensors

Vinafix.com



+V3.3AL  +V3.3AL (11,42,50,51,58,60)

		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: LID		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	38 of 81



		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date: Tuesday, September 26, 2017		Sheet 39 of 81

Vinafix.com



		Project:	330S-KBL Series
		Engineer:	Luffy
Size	Title: NA		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	40 of 81

Wed Jun 03 11:22:59 2015

D

D

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C

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B

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Vinafix.com



INTERNAL ONLY

BPAGE DRAWING

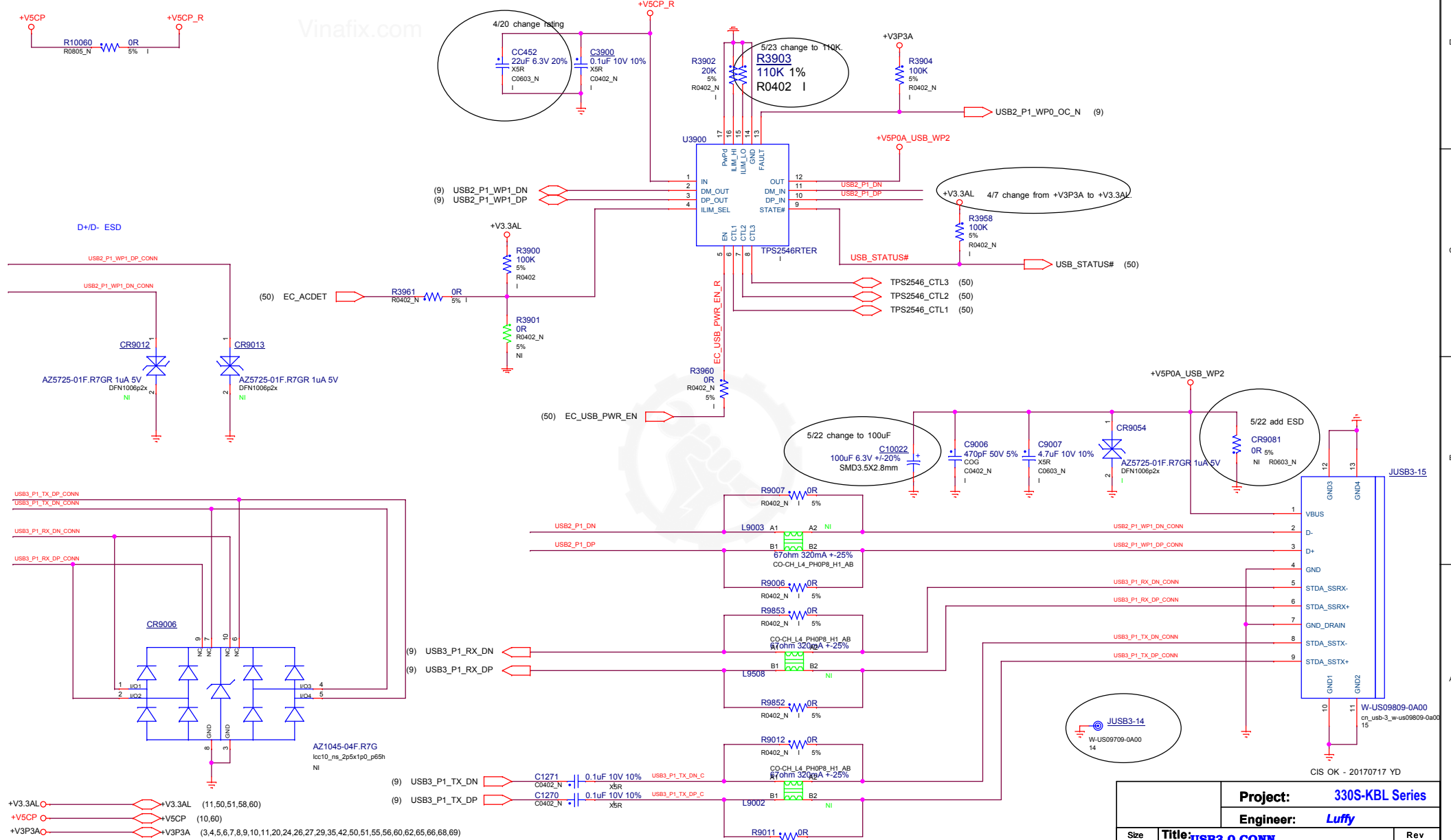
slv_v_mtd-10P3-41
Wed Jun 03 11:22:59 2015

		Project:	330S-KBL Series
		Engineer:	Luffy
Size	Title: NA	Rev	
Custom		V01	
Date:	Tuesday, September 26, 2017	Sheet	41 of 81

USB3.0

Vinafix.com

+V5P0A (10,11,24,27,50,54,61,62,63,65,66,67,68,69,70,72)
 +V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,66,68,69)



Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title: USB3.0 CONN		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	42 of 81

CIS OK - 20170717 YD

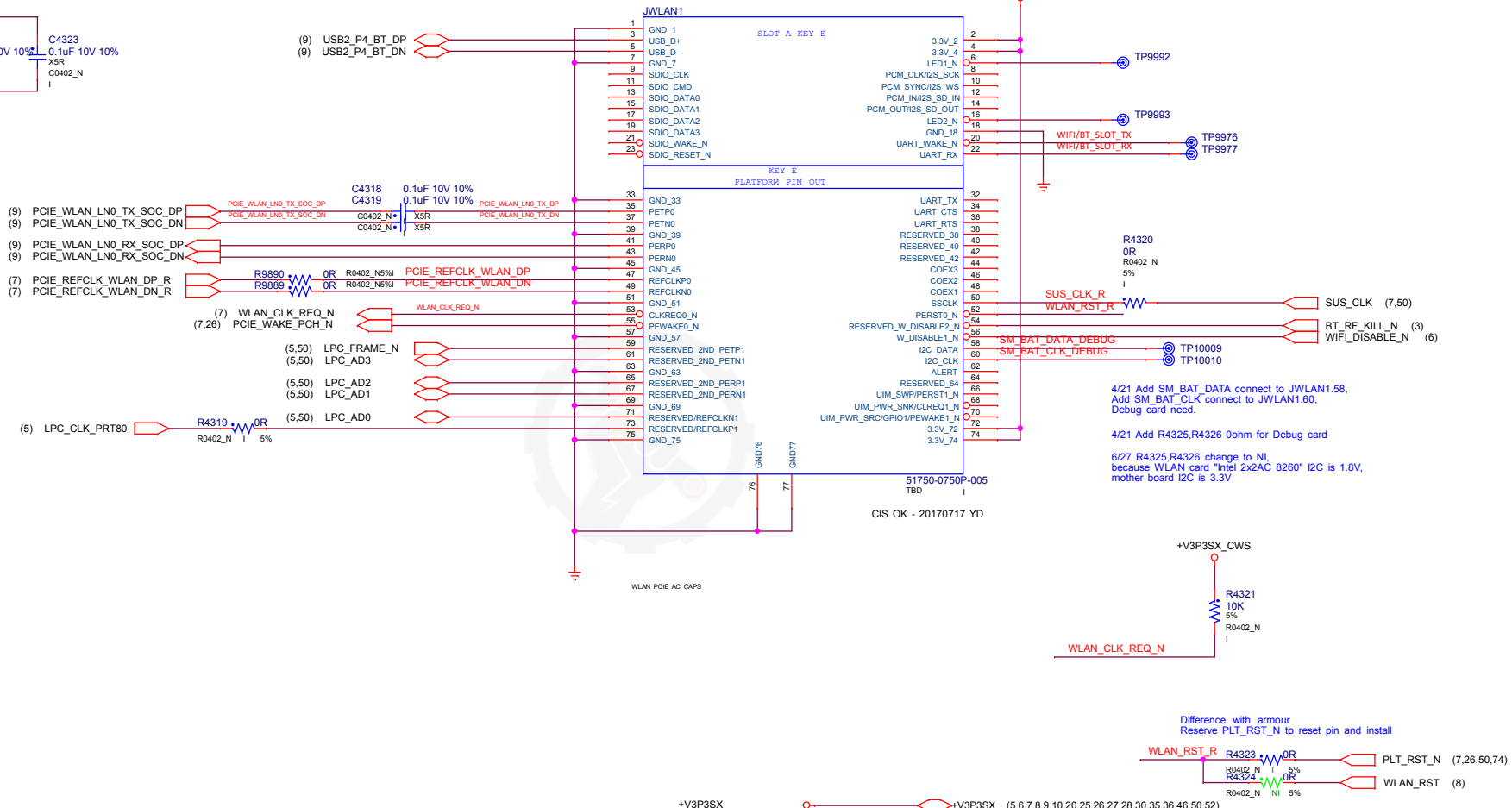
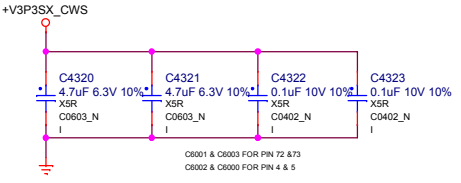
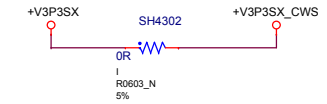
WIFI & BT Module

Vinafix.com

2/16 change CONN

THIS DESIGN SUPPORTS STONE PEAK ONLY

CIS ok



- 4/21 Add SM_BAT_DATA connect to JWLAN1.58, Add SM_BAT_CLK connect to JWLAN1.60, Debug card need.
- 4/21 Add R4325, R4326 0ohm for Debug card
- 6/27 R4325, R4326 change to NI, because WLAN card "Intel 2x2AC 8260" I2C is 1.8V, mother board I2C is 3.3V

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: WLAN WIFI BT MODULE
Date: Tuesday, September 28, 2017	Rev: V01
Sheet 43 of 81	

INTERNAL ONLY

BPAGE DRAWING

slv_y_mtd-10P3-43
Wed Jun 03 11:23:00 2015

Vinafix.com



		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date:	Tuesday, September 26, 2017	Sheet 44 of 81

D

D

C

C

B

B

A

A

Vinafix.com

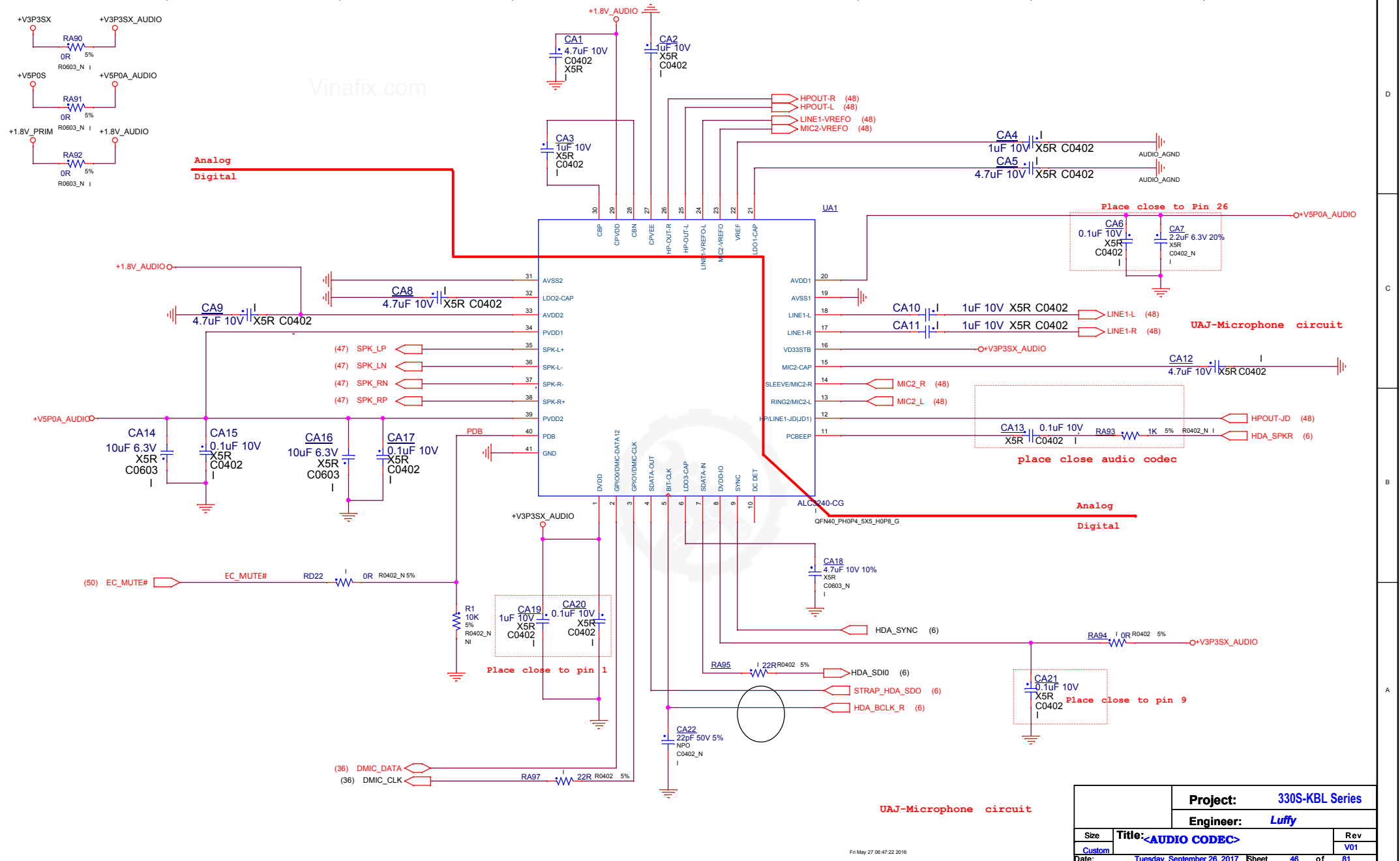


INTERNAL ONLY

BPAGE DRAWING

skv_y_mid.GND
Wed Jun 03 11:23:01 2015

		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
Custom		V01
Date: Tuesday, September 26, 2017	Sheet 45	of 81

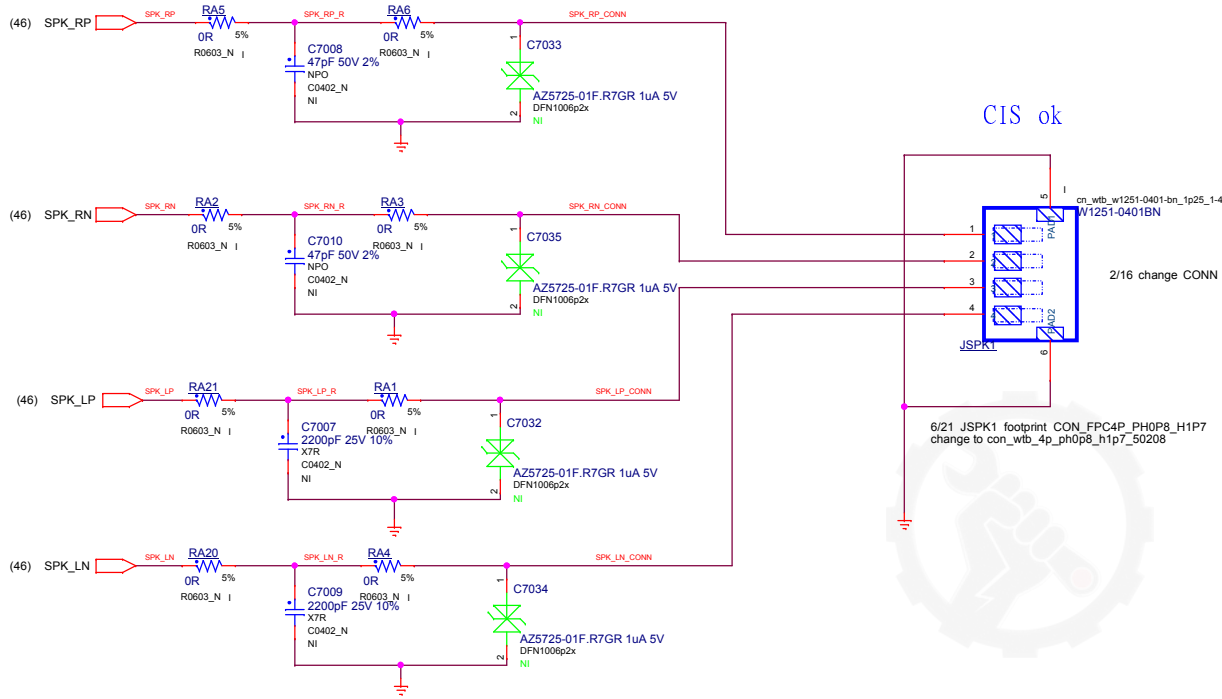


UAJ-Microphone circuit

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: <AUDIO CODEC>
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 46	of: 81

Speaker

Vinafix.com



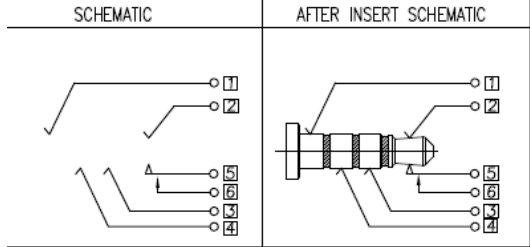
INTERNAL ONLY

BPAGE DRAWING
 sky_y_mtd.GND
 Wed Jun 03 11:23:02 2015

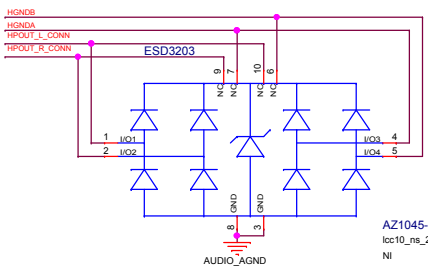
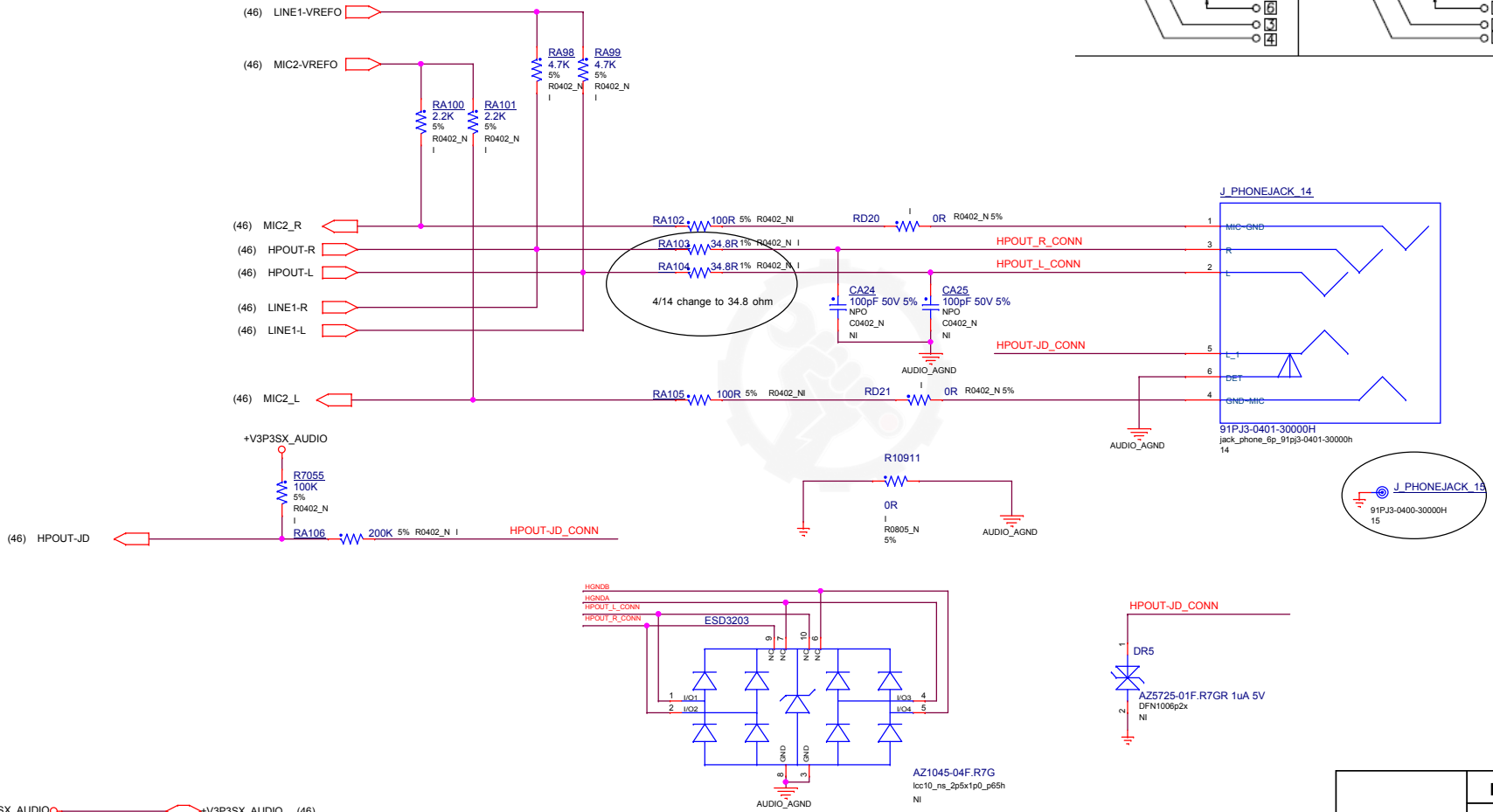
		Project: 330S-KBL Series	
		Engineer: Luffy	
Size	Title: Speaker		Rev
Custom			V01
Date:	Tuesday, September 26, 2017	Sheet	47 of 81

HEADSET JACK (Supports CTIA and OMTP headsets)

Important:
 To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.



Vinafix.com



AZ1045-04F.R7G
 lcc10_ns_2p5x1p0_p65h
 NI

INTERNAL ONLY

BPAGE DRAWING

REV: 01.0A
 Fri May 27 06:47:24 2016

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: <AUDIO HEADSET>
Date: Tuesday, September 26, 2017	Rev: V01
Sheet 48 of 81	

Vinafix.com

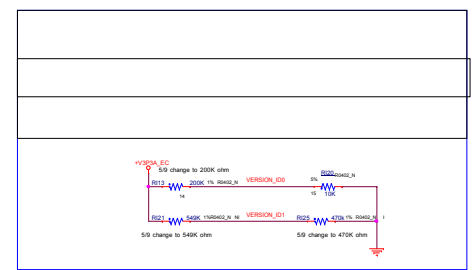
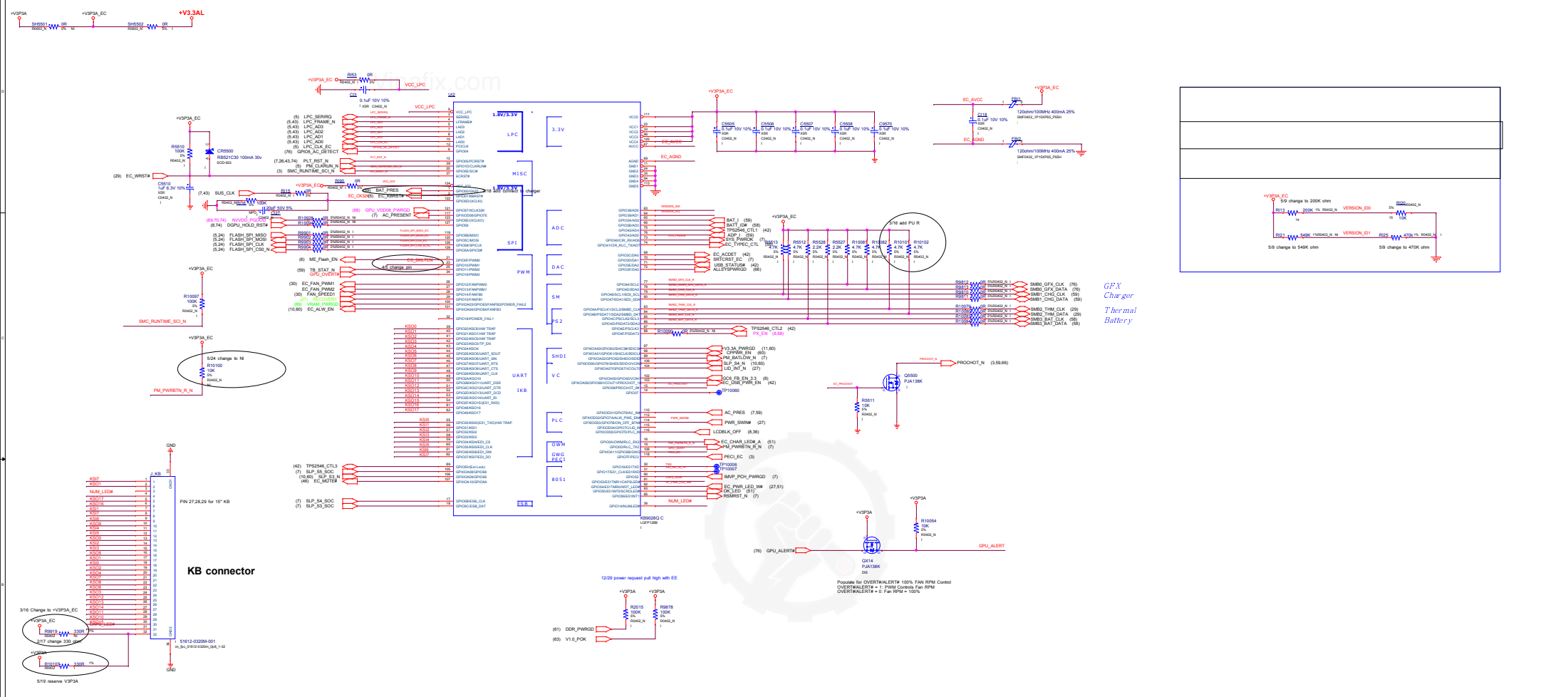


BPAGE DRAWING

skv_y_mrd +VCHG.49
Wed Jun 03 11:23:03 2015

		Project:	330S-KBL Series
		Engineer:	Luffy
Size	Title:	NA	
Custom			Rev
			V01
Date:	Tuesday, September 26, 2017	Sheet	49 of 81

EC controller

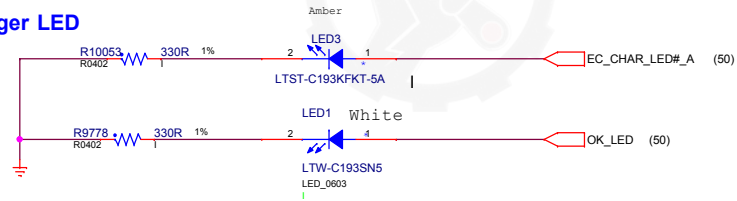


GFY Charger
Thermal Battery

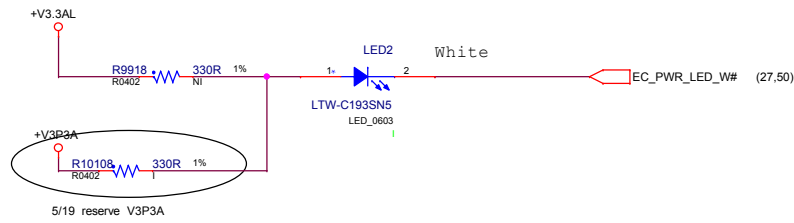
20170718 yangzw genghuan

Project: 330S-KBL	
Engineer: Linyi	
Size: A	Title: EMBEDDED CONTROLLER
Rev: 1	Ver: 1
Date: 2016-08-26 10:17	Sheet: 20 of 21

Charger LED

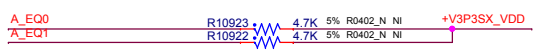
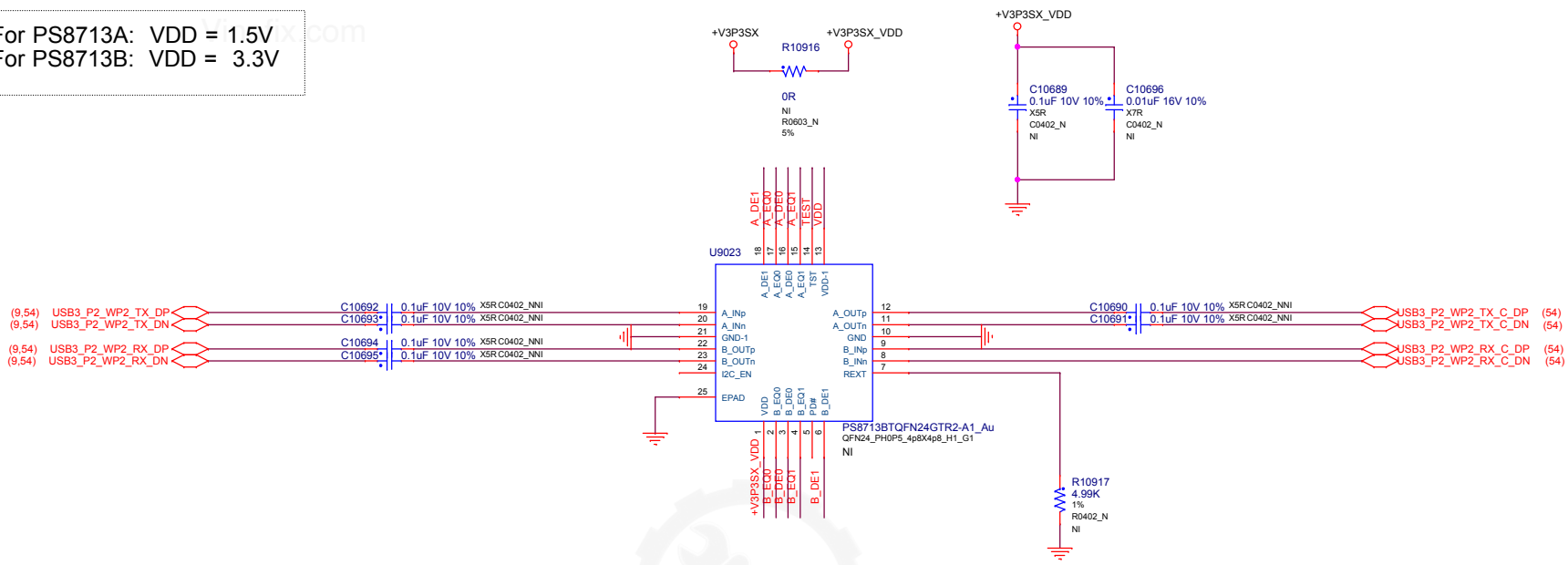


SYS LED

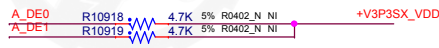


		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: BUTTON & LED	Rev
Custom		V01
Date:	Tuesday, September 26, 2017	Sheet 51 of 81

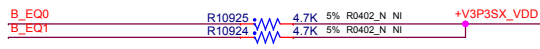
For PS8713A: VDD = 1.5V
 For PS8713B: VDD = 3.3V



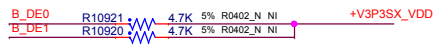
Equalizer control and program for channel A
 3.3V tolerant. Internally pulled down at ~150KΩ
 [A_EQ1, A_EQ0] ==
 LL: program EQ for channel loss up to 9.5dB(default)
 LH: program EQ for channel loss up to 13dB
 HL: program EQ for channel loss up to 4.5dB
 HH: program EQ for channel loss up to 7.5dB



Programmable output pre-emphasis level setting for channel A
 3.3V tolerant. Internally pulled down at ~150KΩ
 [A_DE1, A_DE0] ==
 LL: 3.5dB de-emphasis
 LH: No de-emphasis
 HL: 2.7dB de-emphasis
 HH: 5dB de-emphasis



Equalizer control and program for channel B
 3.3V tolerant. Internally pulled down at ~150KΩ
 [B_EQ1, B_EQ0] ==
 LL: program EQ for channel loss up to 9.5dB(default)
 LH: program EQ for channel loss up to 13dB
 HL: program EQ for channel loss up to 4.5dB
 HH: program EQ for channel loss up to 7.5dB

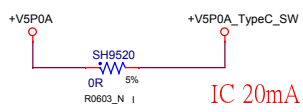


Programmable output pre-emphasis level setting for channel B
 3.3V tolerant. Internally pulled down at ~150KΩ
 [B_DE1, B_DE0] ==
 LL: 3.5dB de-emphasis
 LH: No de-emphasis
 HL: 2.7dB de-emphasis
 HH: 5dB de-emphasis

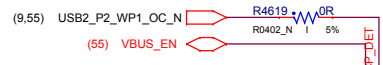


LFPS swing adjust
 3.3V tolerant. Internally pulled down at ~150KΩ.
 TEST ==
 L: Normal LFPS swing (default)
 H: Turn down LFPS swing

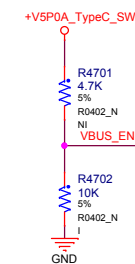
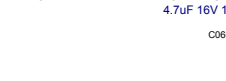
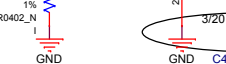
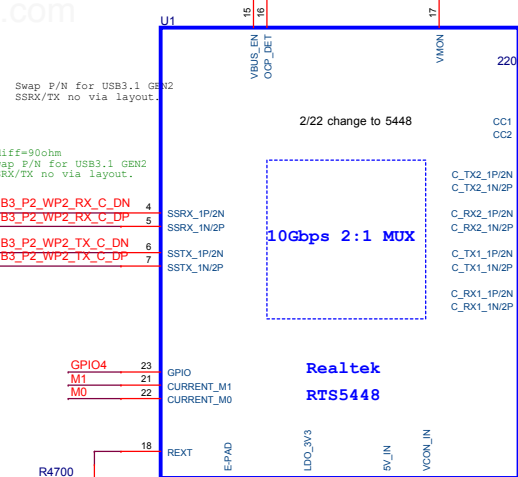
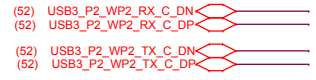
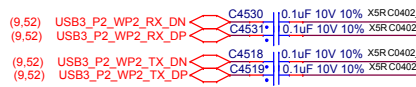
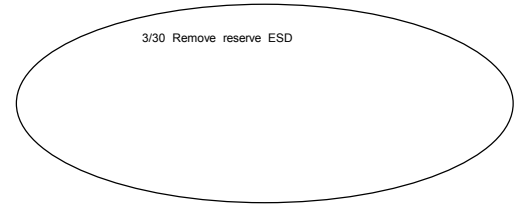
Project: 330S-KBL Series		Rev
Engineer: Luffy		V01
Size: Custom	Title: TYPE-C Switch	Date: Tuesday, September 26, 2017
Sheet 52 of 81		



IC 20mA



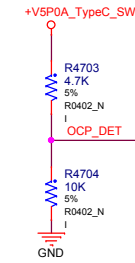
Vinafix.com



Power Switch High Enable

Power switch enable pin	Note
Low Active	R4701/R4702 mount
High Active	R4702 mount,R16 don't mount

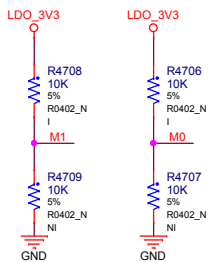
For C_VBUS power switch enable pin



OCP Low Enable

Power switch OCP pin	Note
Low Active	R4704/R4703 mount
High Active	R4704 mount,R4703 don't mount

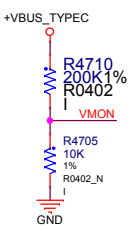
For C_VBUS power switch OCP pin



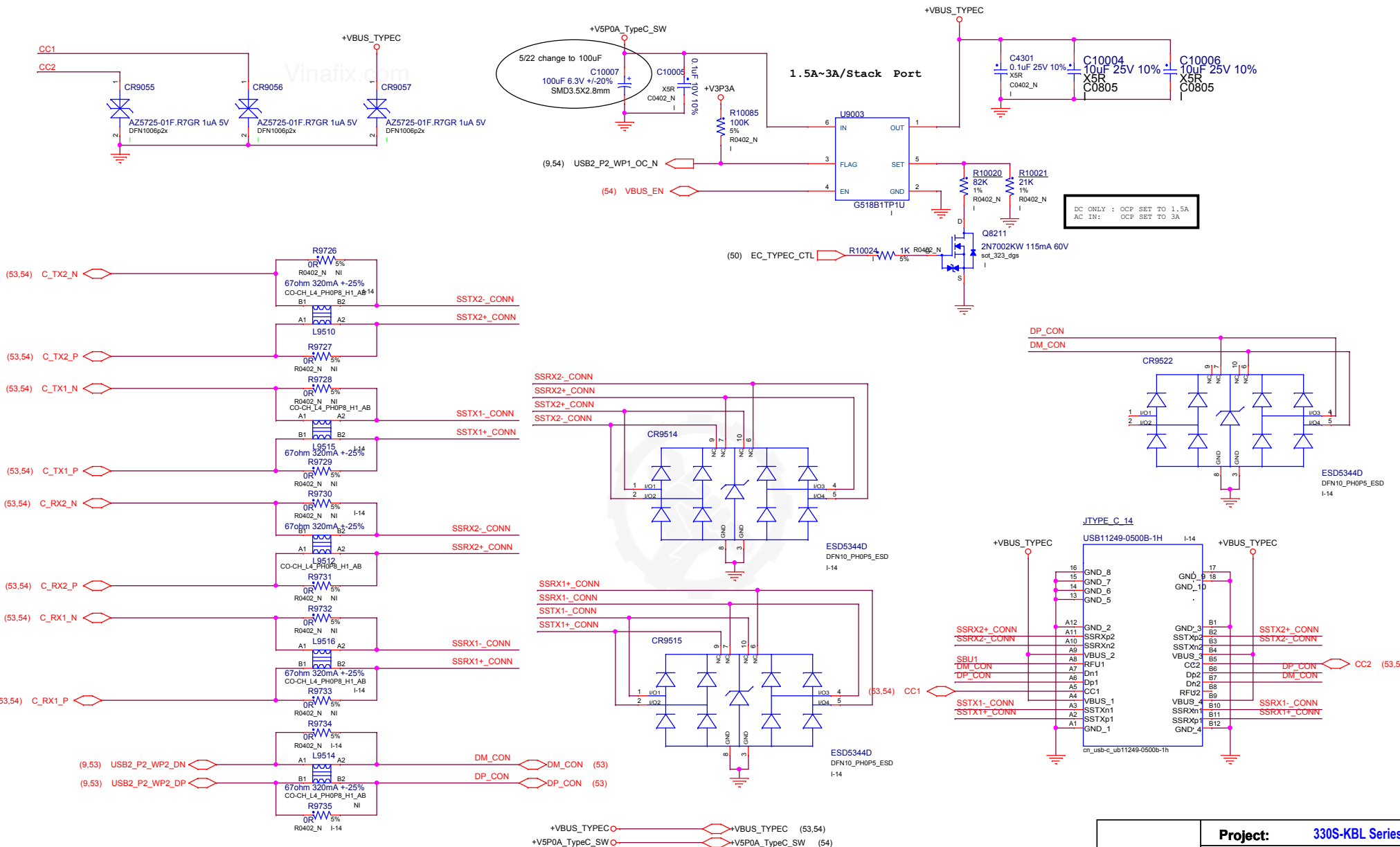
Rp	M1	M0	Note
Rp: 900mA	0	1	R11/R12 mount,R10/R13 don't mount
Rp: 1.5A	1	0	R10/R13 mount,R11/R12 don't mount
Rp: 3.0A	1	1	R10/R12 mount,R11/R13 don't mount

Rp: 1.5A (now)

Rp configuration



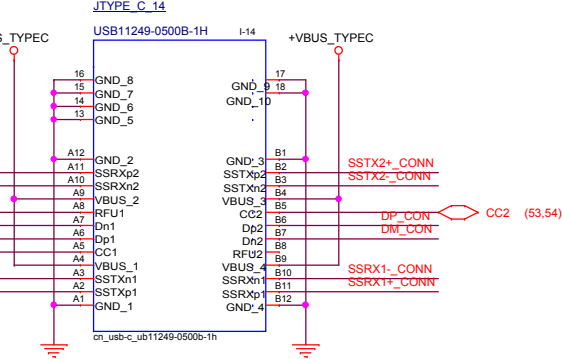
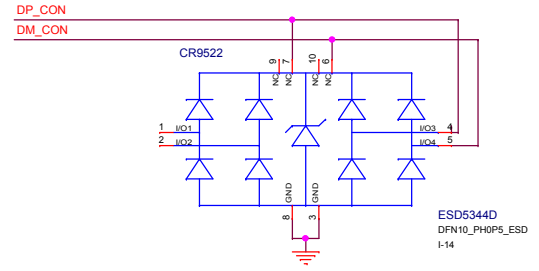
Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: TYPE-C Switch
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 54	of 81



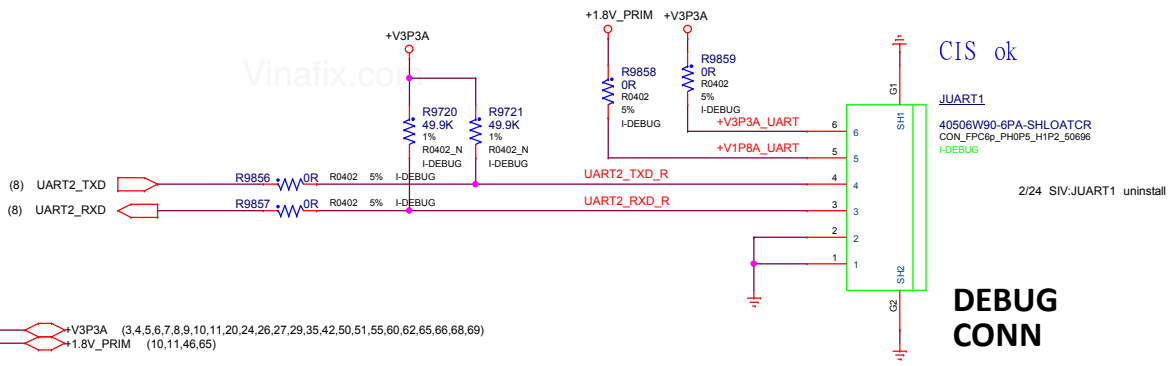
DC ONLY : OCP SET TO 1.5A
AC IN : OCP SET TO 3A

5/22 change to 100uF
C10007
100uF 6.3V +/-20%
SMD3.5X2.8mm

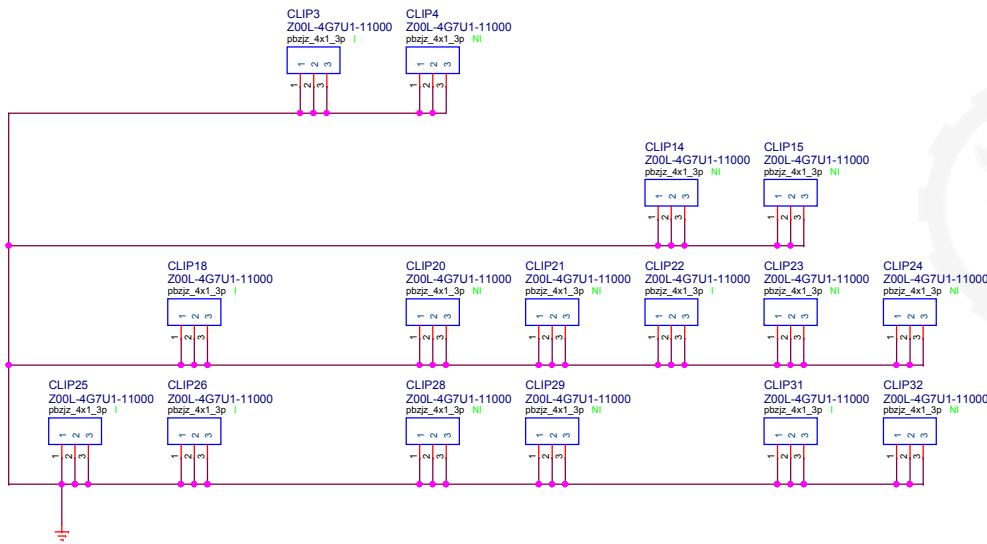
1.5A-3A/Stack Port



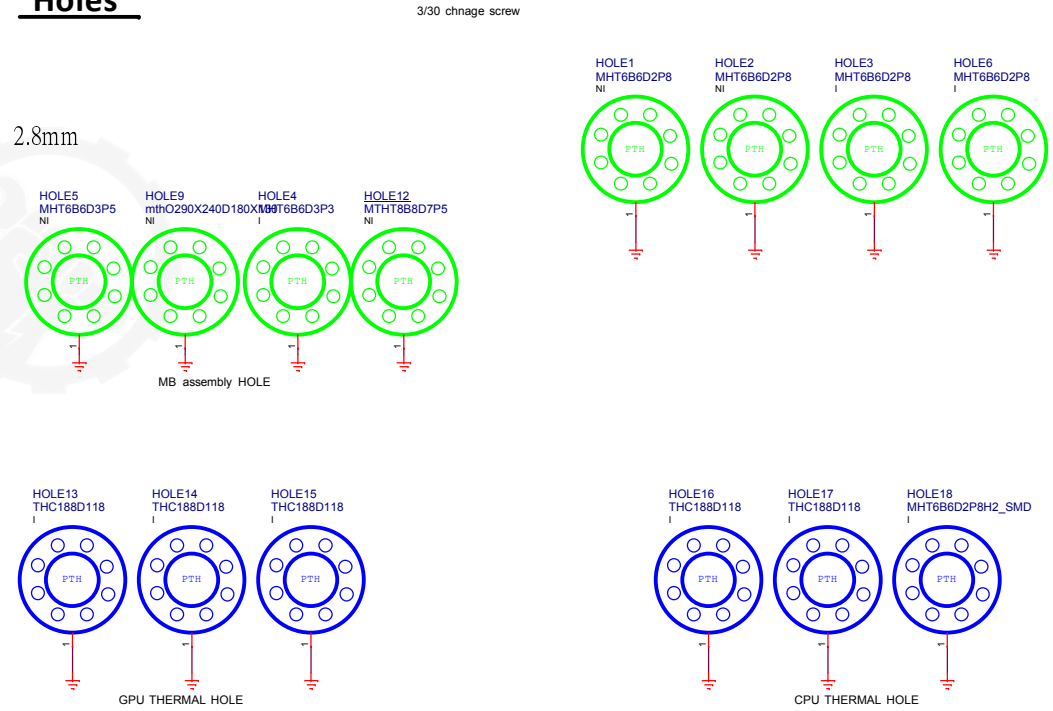
Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: TYPE-C CONN
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 55	of 81



Shielding



Holes



Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: UART CONN & HOLE & CLIP
Date: Tuesday, September 26, 2017	Rev: V01
Sheet 56 of 81	

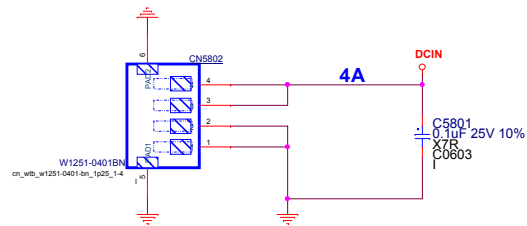
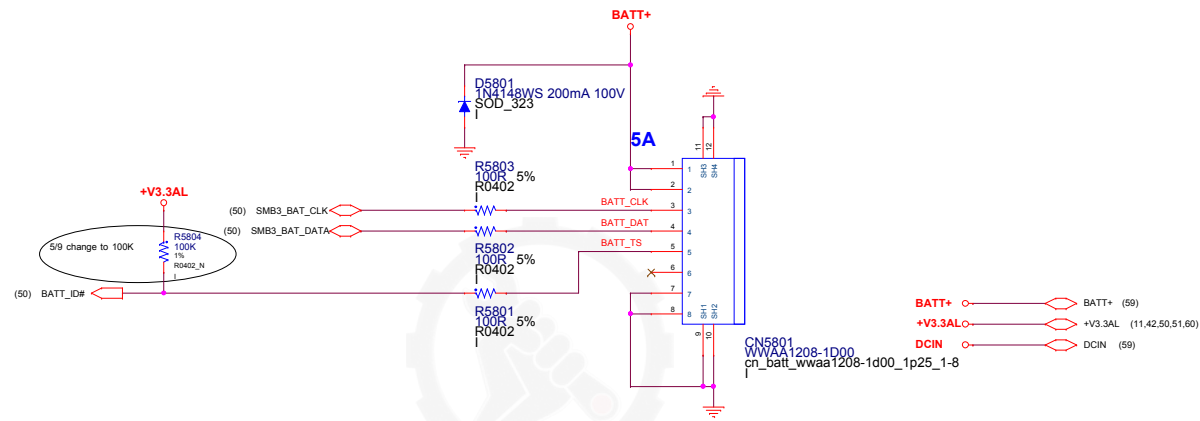
EVT=>SIV

- No. Change details Change Reason
- 1 LID_INT_N change PU to +V3.3AL. EC need recognize LID in S5.
 - 2 Change KBL_CONN Pin define. EVT CE not confirm the Pin define correct.
 - 3 Change Touch PAD Pin define. Touch PAD SPEC update, add LID control Pin.
 - 4 Change Keyboard power LED voltage to +V3.3AL. Synchronize with System LED.
 - 5 Type C IC Pin.20 change to LDO_3V3. LDO_3V3 lose connection.
 - 6 Install RS74_RS57. Install for GPU.
 - 7 remove DR3_DR4. unnecessary
 - 8 Change USB2 solution. for support 1V voltage
 - 9 Add PU for SMB2_THM_CLK_DATA. lose SMB PU
 - 10 remove C10026. unnecessary



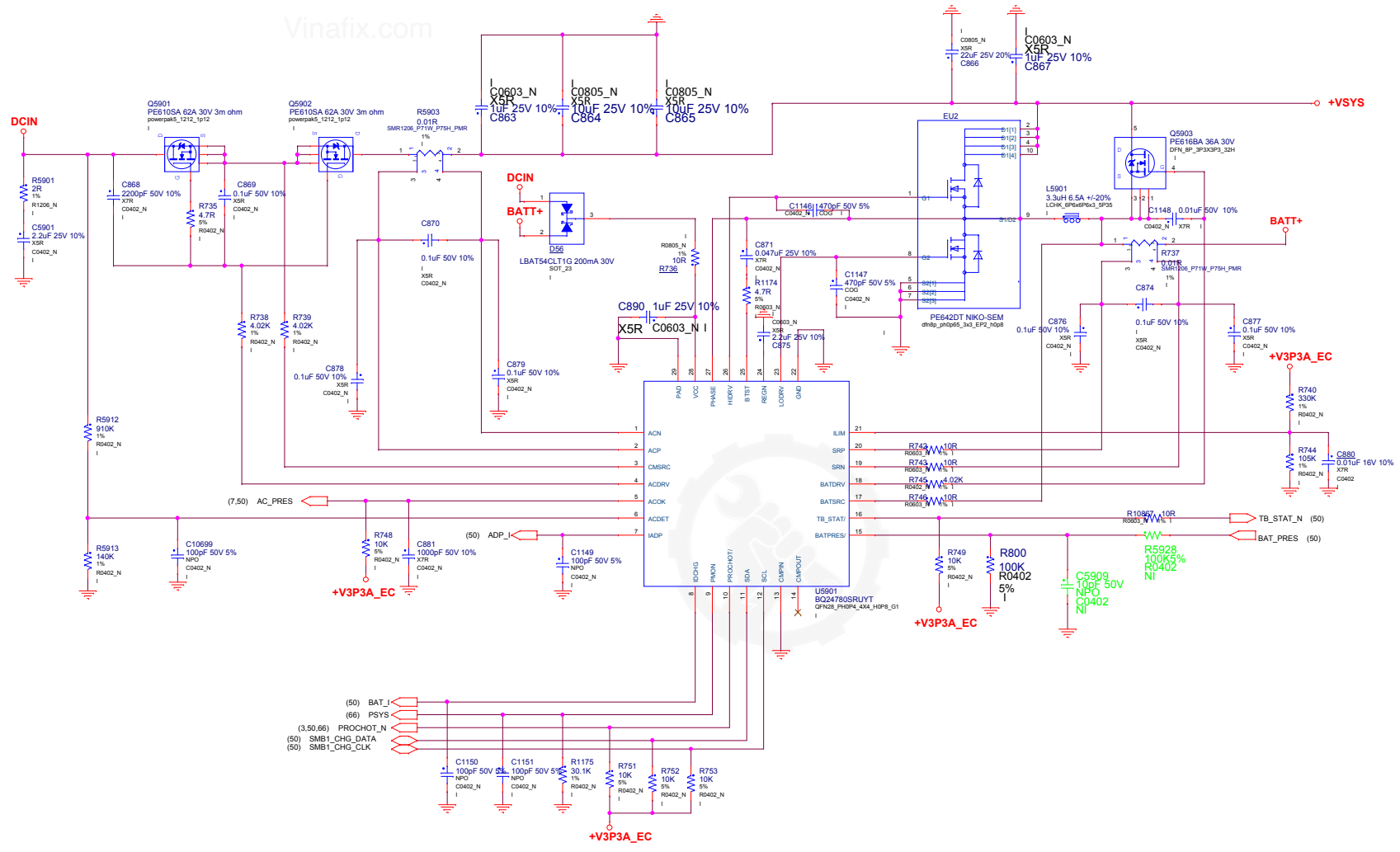
		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title:	Rev
C	HW Change List	V01
Date:	Tuesday, September 26, 2017	Sheet 57 of 81

58: BATTERY CONNECTOR



59: BATTERY CHARGER

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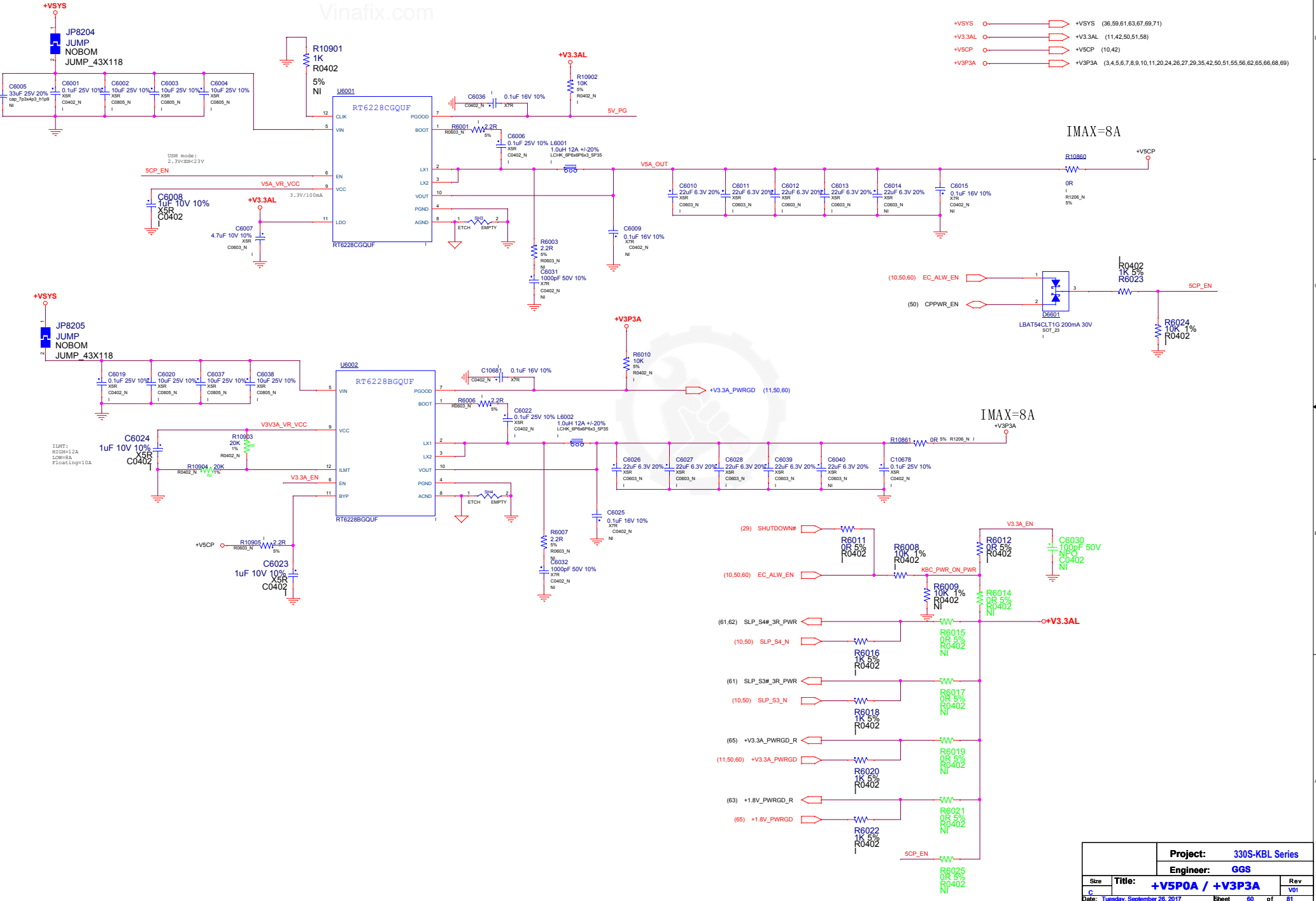


Project: 330S-KBL Series	
Engineer: GGS	
Size: C	Title: CHARGER
Date: Wednesday, September 27, 2017	Rev: v01
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60: +V5P0A / +V3P3A POWER SUPPLY

Vinafix.com

- +V5YS (36,59,61,63,67,69,71)
- +V3.3AL (11,42,50,51,58)
- +V5CP (10,42)
- +V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,62,65,66,68,69)

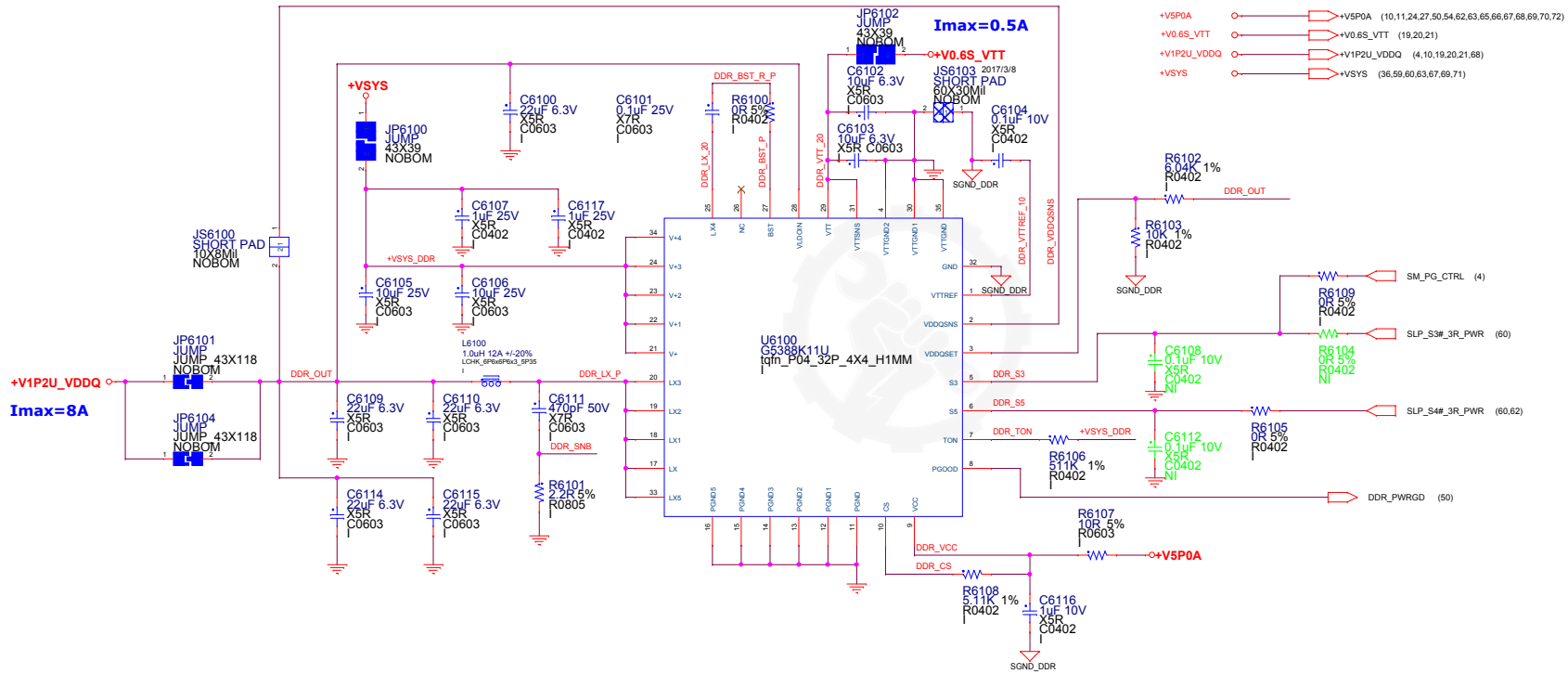


IMAX=8A

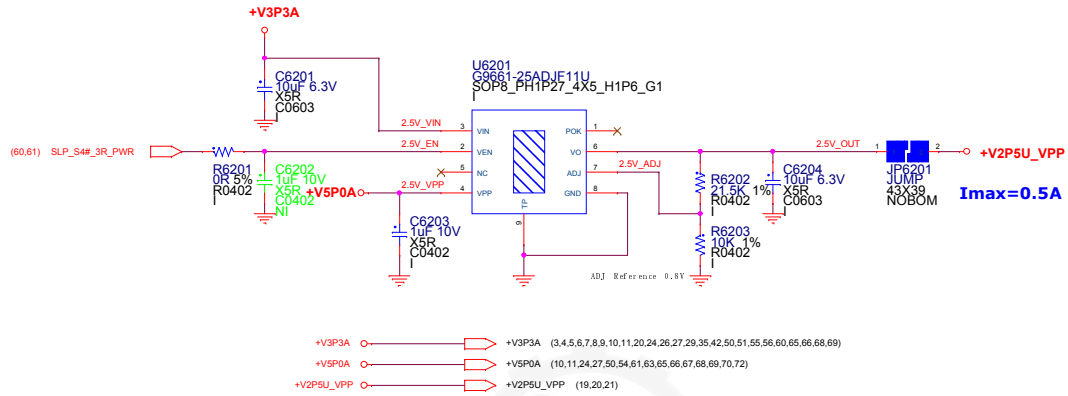
IMAX=8A

Project: 330S-KBL Series		Rev
Engineer: GGS		V01
Size	Title: +V5P0A / +V3P3A	Rev
C	Date: Tuesday, September 26, 2017	Sheet 60 of 81

61: DDR POWER SUPPLY

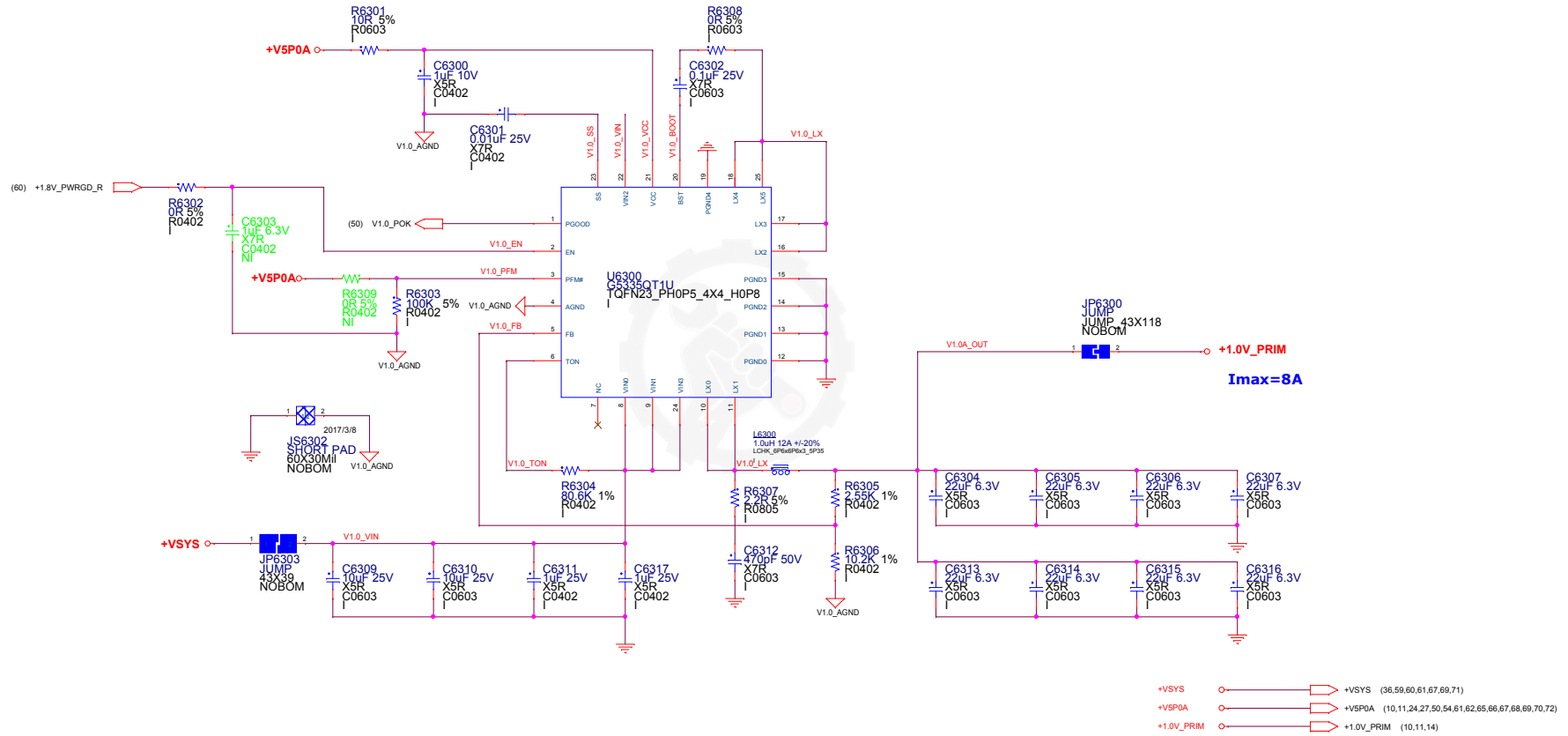


62: +V2P5U_VPP POWER SUPPLY



Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title:		Rev
C	+V2P5U_VPP		V01
Date: Tuesday, September 26, 2017		Sheet	62 of 81

63: +1.0V_PRIM POWER SUPPLY

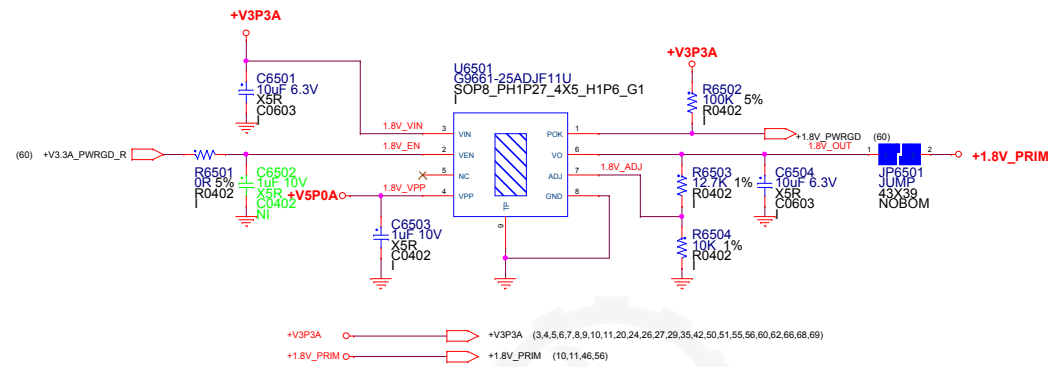


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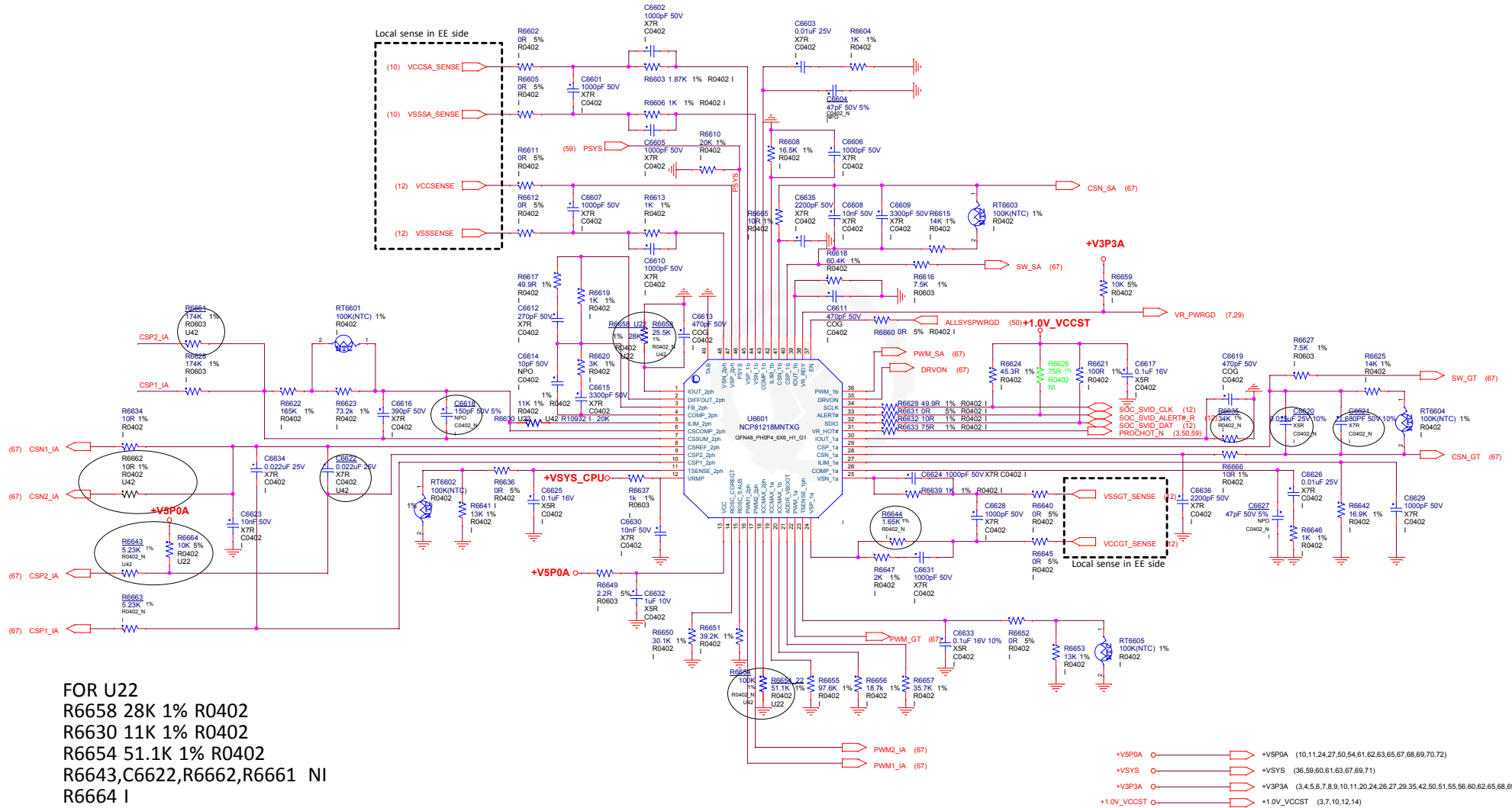


		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: NA	Rev
C		V01
Date: Tuesday, September 26, 2017		Sheet 64 of 81

65: +1.8V_PRIM POWER SUPPLY



66: CPU POWER SUPPLY



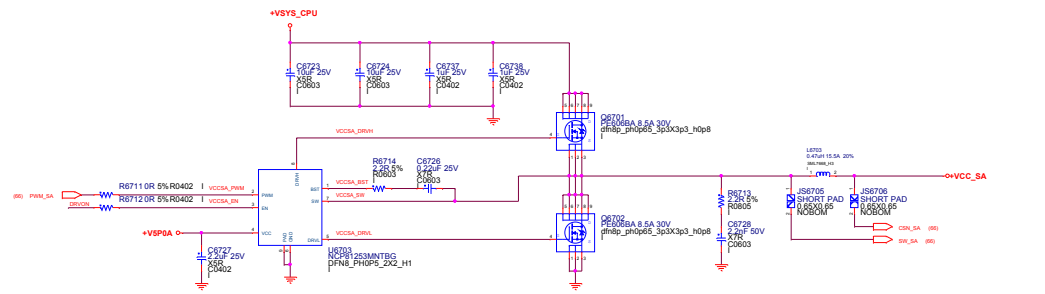
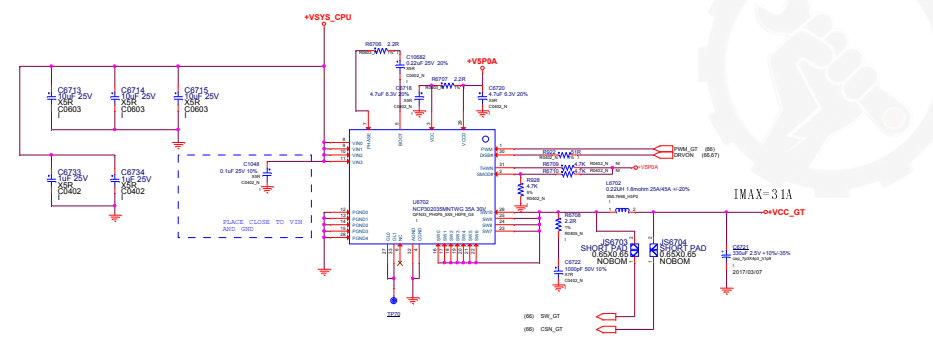
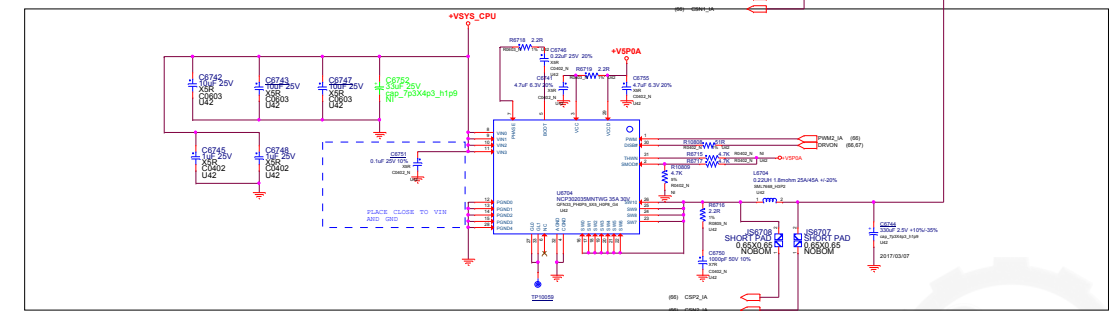
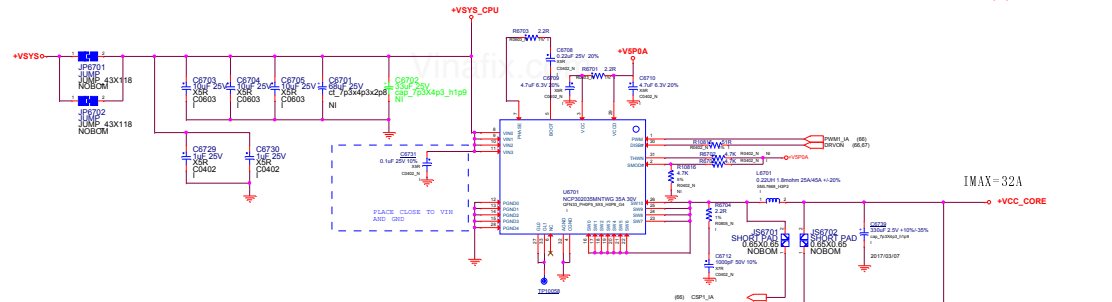
- FOR U22
 R6658 28K 1% R0402
 R6630 11K 1% R0402
 R6654 51.1K 1% R0402
 R6643,C6622,R6662,R6661 NI
 R6664 I
 C6744 NI

- +V5P0A (10,11,24,27,50,54,61,62,63,65,67,68,69,70,2)
- +V5YS (36,59,60,61,63,67,69,71)
- +V3P3A (3,4,5,6,7,8,9,10,11,20,24,26,27,29,35,42,50,51,55,56,60,62,65,68,69)
- +1.0V_VCCST (3,7,10,12,14)

Project: 330S-KBL Series		Rev	
Engineer: Luffy		V01	
Title: CPU VR IC	Date: Tuesday, September 26, 2017	Sheet 66	of 81

67: VCC_CORE/GT/SA POWER SUPPLY

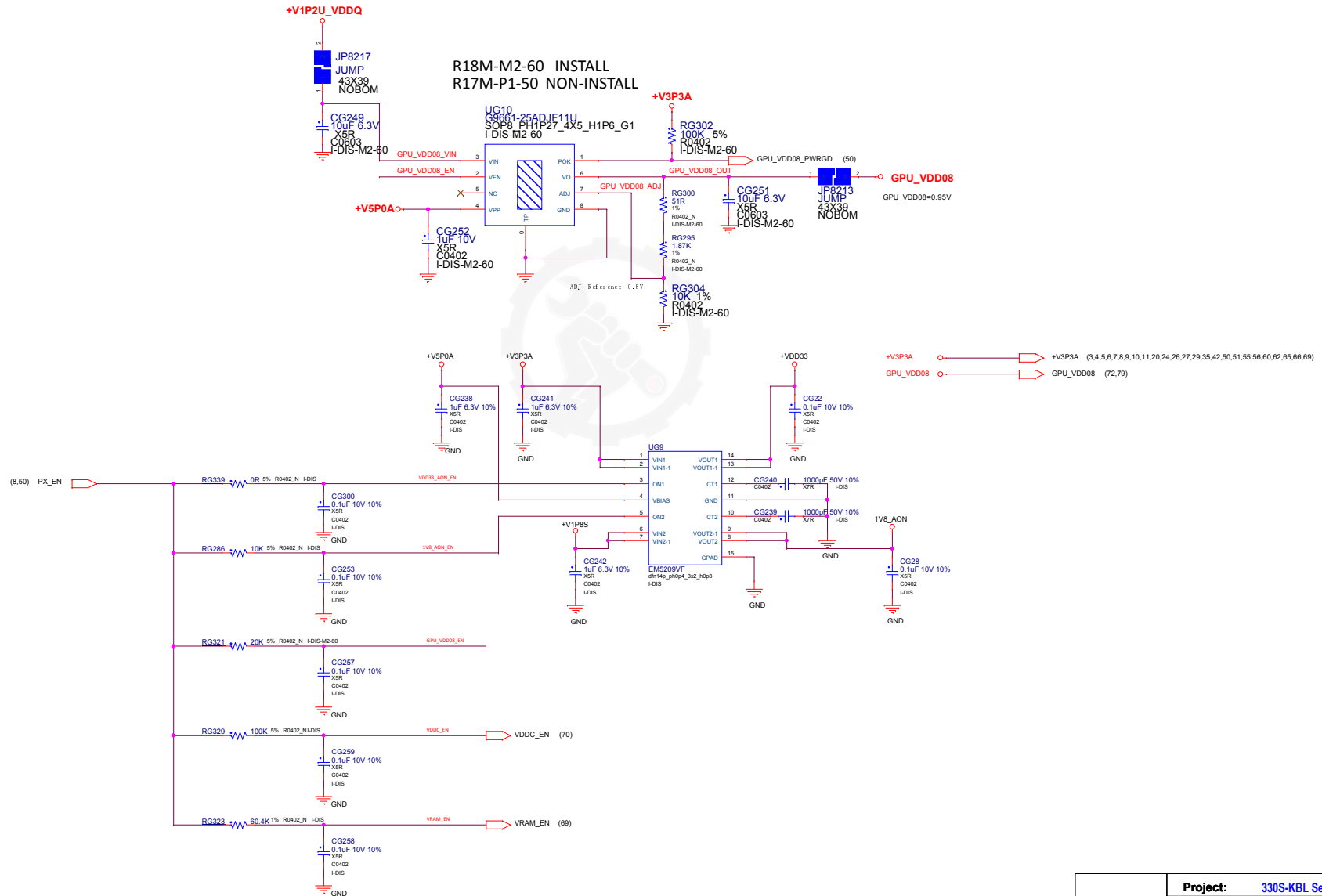
- +VSYS CPU → +VSYS_CPU (0.0, 0.0, 0.0, 0.0, 0.0)
- +VSYS CPU → +VSYS_CPU (0.0)
- +VSPDA → +VSPDA (10.11, 24.27, 20.54, 0.1, 0.2, 0.3, 0.5, 0.6, 0.8, 0.9, 7.0, 7.1)
- +VCC_CORE → +VCC_CORE (12.15, 2.3)
- +VCC_GT → +VCC_GT (12.15)
- +VCC_SA → +VCC_SA (15.15)



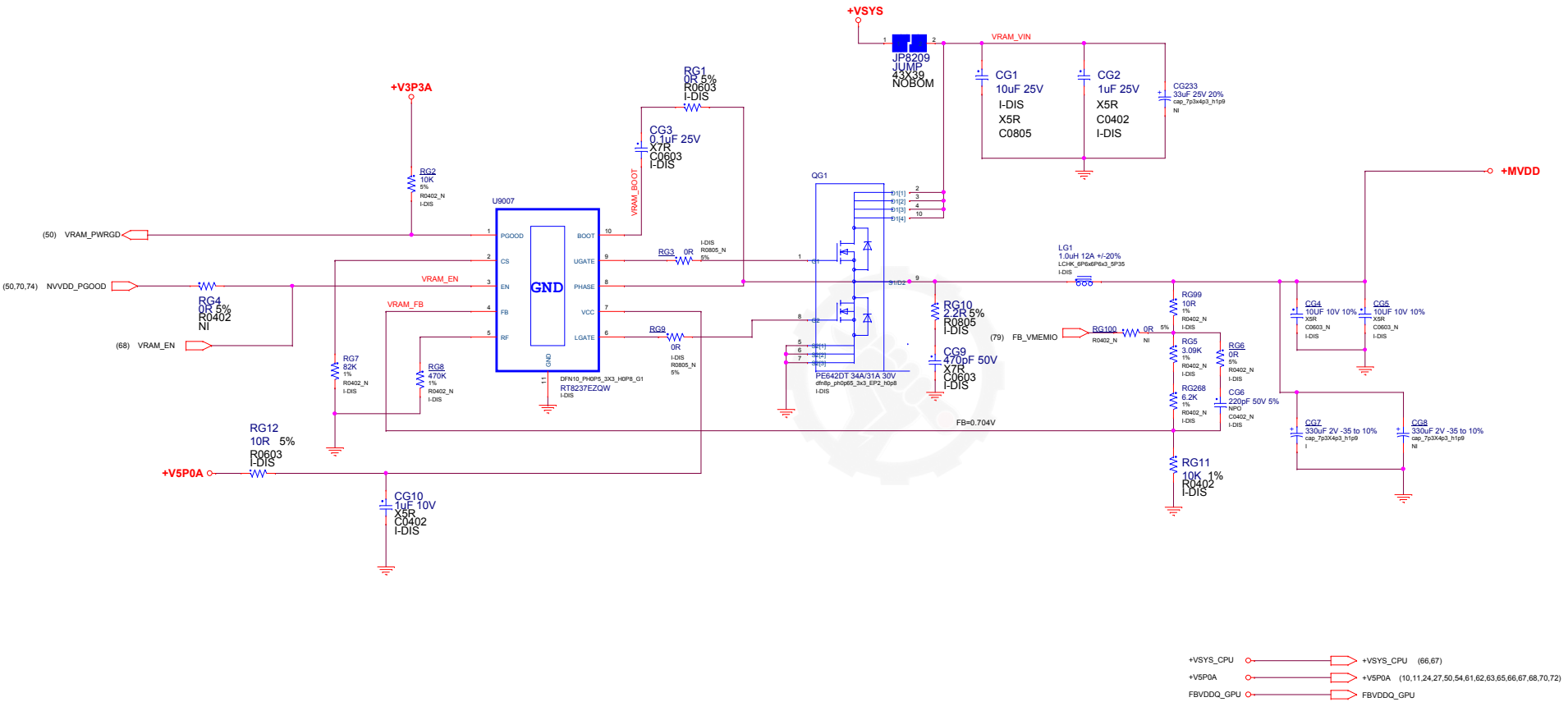
Project:	330S-KBL Series
Engineer:	Luffy
Rev:	1
Title:	VCC_CORE/GT/SA
Sheet:	1 of 1

VDD POWER SUPPLY for M2-60

Vinafix.com

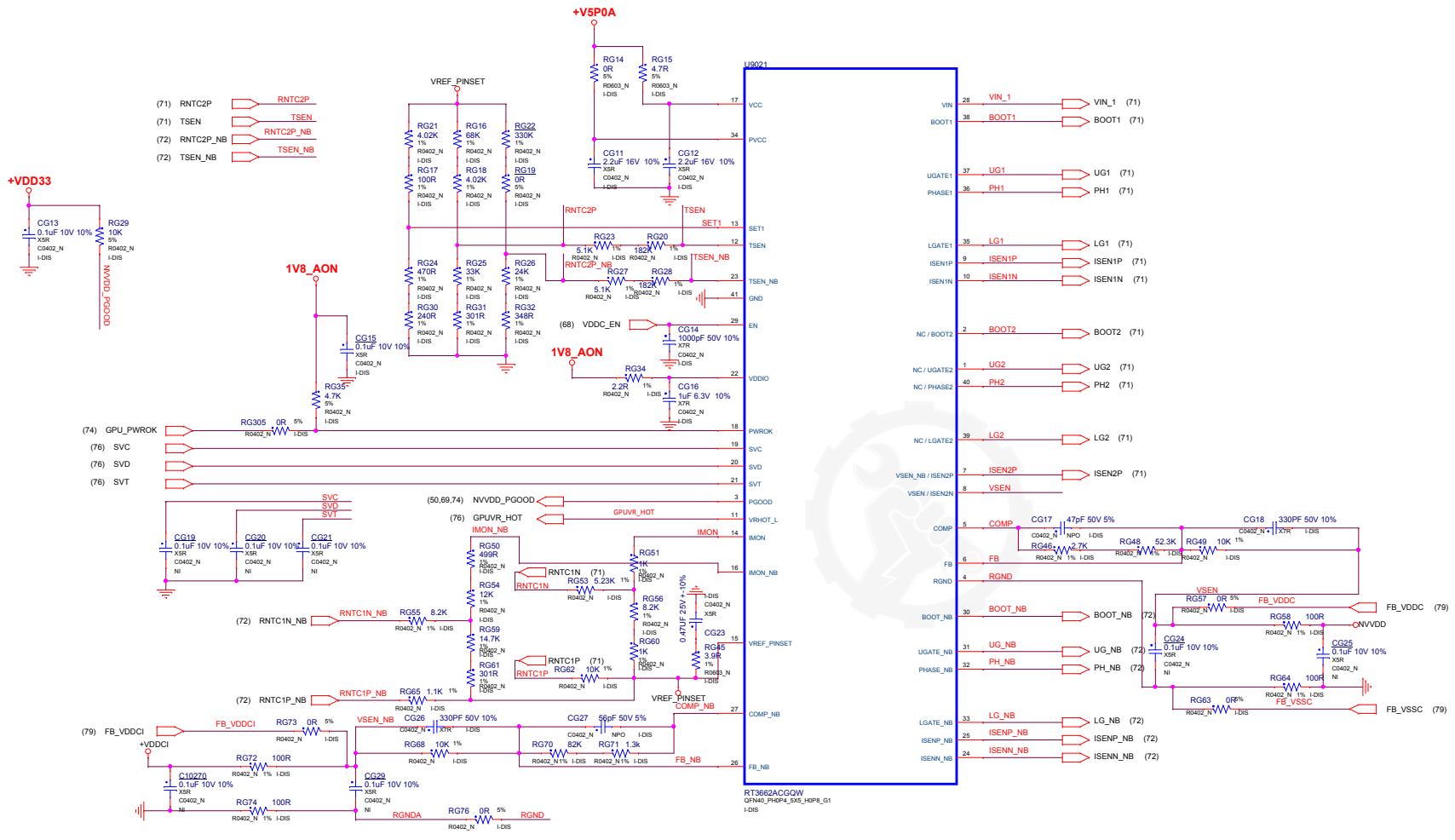


Project: 330S-KBL Series	
Engineer: Luffy	
Size: C	Title: GPU-VDD08
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 68	of 81

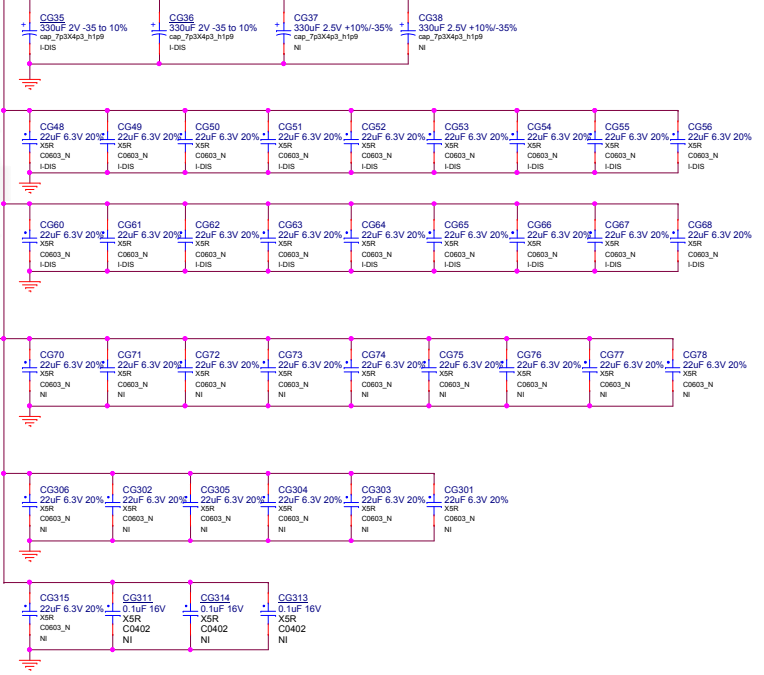
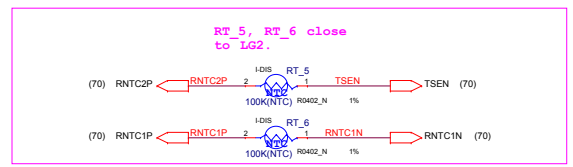
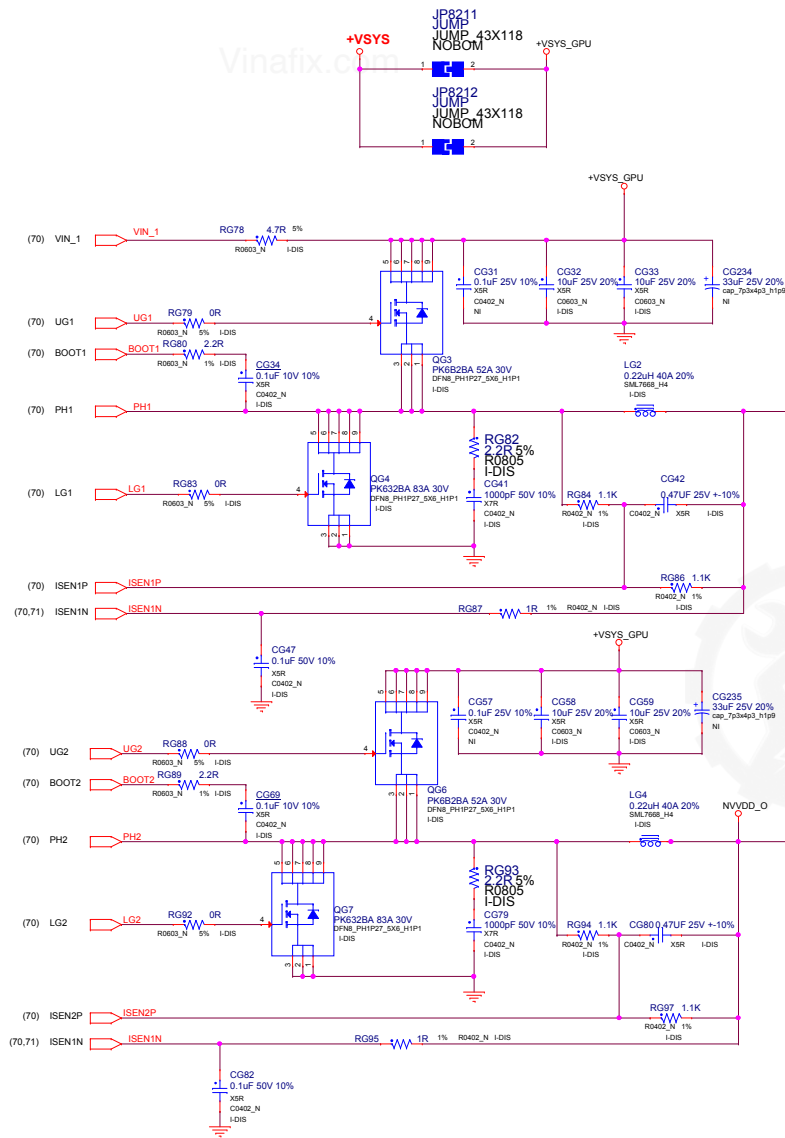


70: GPU POWER

Vinafix.com

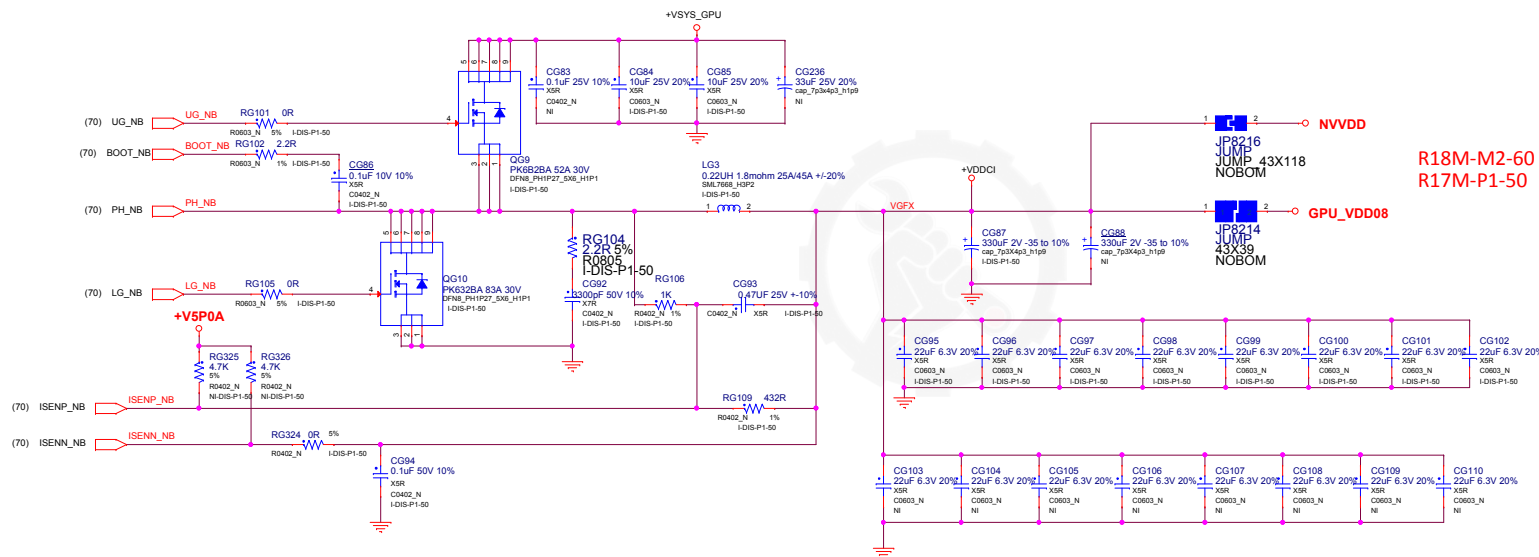
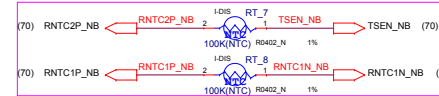


Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title:	Rev	
C	GPU NVVDD	V01	
Date:	Tuesday, September 26, 2017	Sheet	70 of 81



Project: 330S-KBL Series	
Engineer: Luffy	
Size: C	Title: GPU NVDD
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 71	of: 81

RT 7, RT 8 close to LG3.



R18M-M2-60 INSTALL RG325/RG326

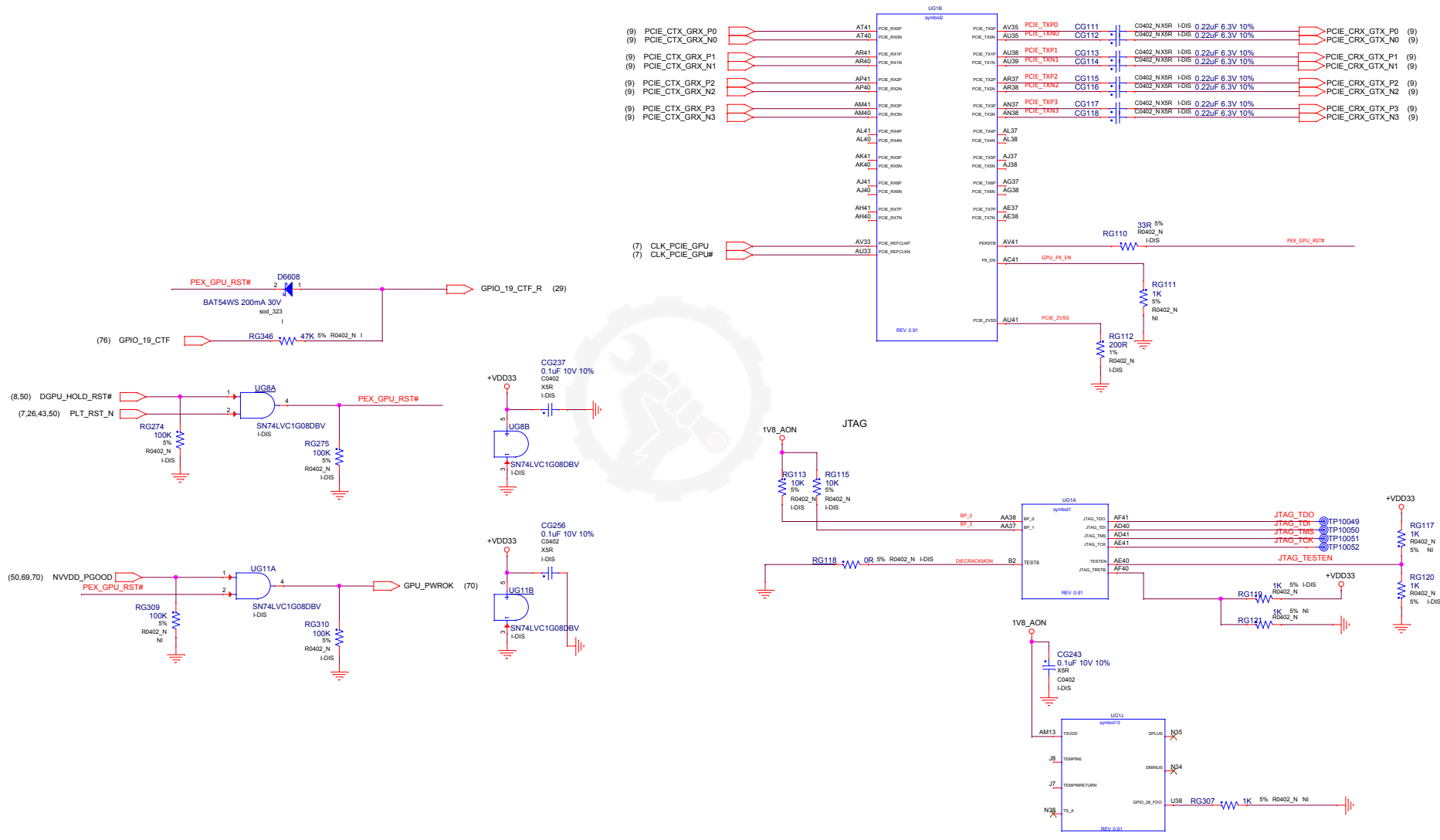
R18M-M2-60 INSTALL JP8216 AND NC this phase
R17M-P1-50 INSTALL JP8214, non-install JP8216

Project: 330S-KBL Series		Rev
Engineer: Luffy		V01
Size	Title: VDDCI	Rev
C		
Date: Tuesday, September 26, 2017	Sheet 72 of 81	

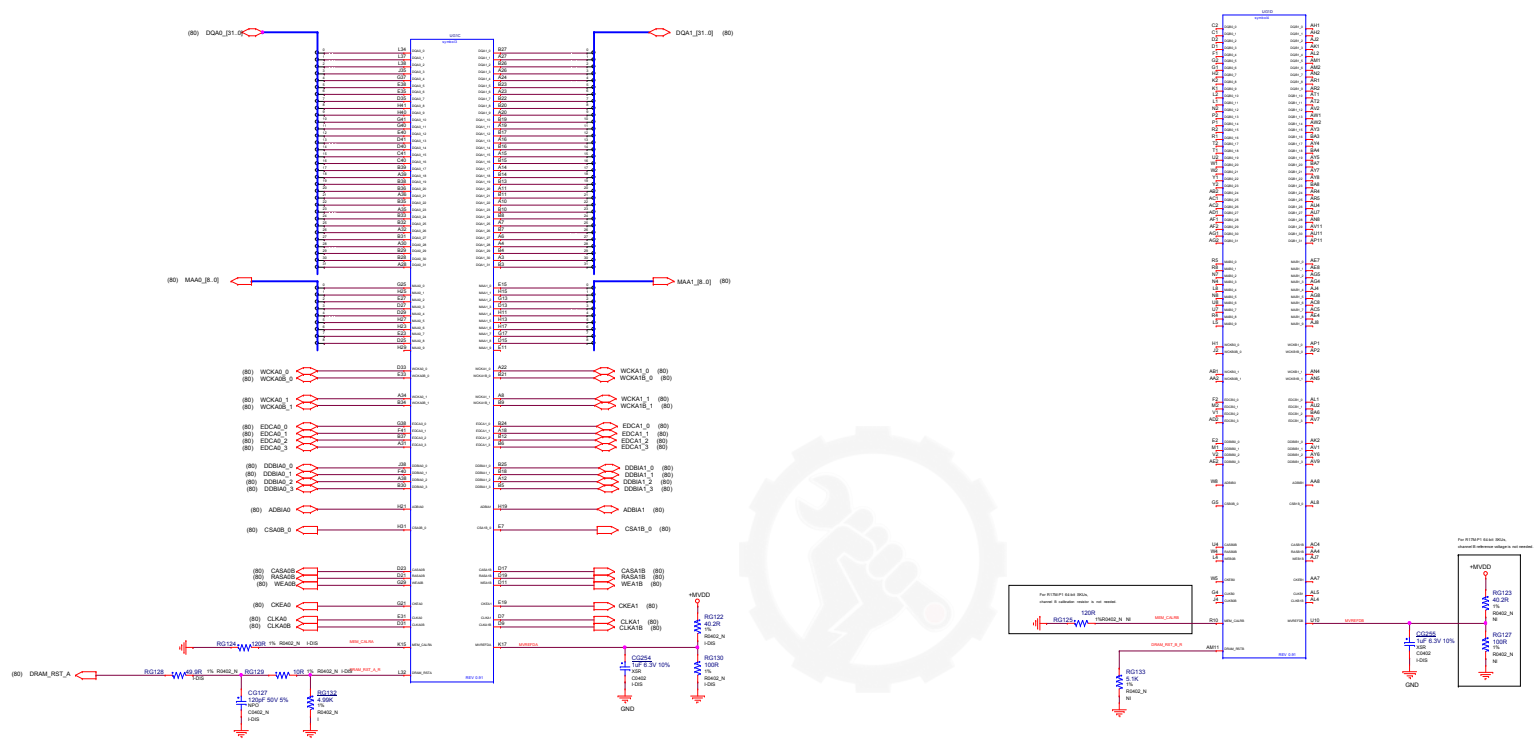
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		Project: 330S-KBL Series
		Engineer: Luffy
Size	Title: POWER MAP	Rev
B		V01
Date: Tuesday, September 26, 2017		Sheet 73 of 81



Project: 330S-KBL Series	
Engineer: Luffy	
Size: Custom	Title: GPU PCIe/DP
Date: Tuesday, September 26, 2017	Rev: V01
Sheet: 74	of: 81

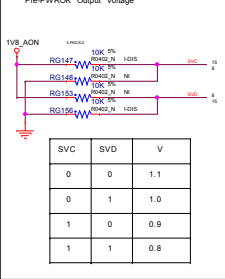


Project: 330S-KBL Series	
Engineer: Luffy	
Drawn: Yida	Checked: MRS
Date: 2024.08.26	Rev: 01

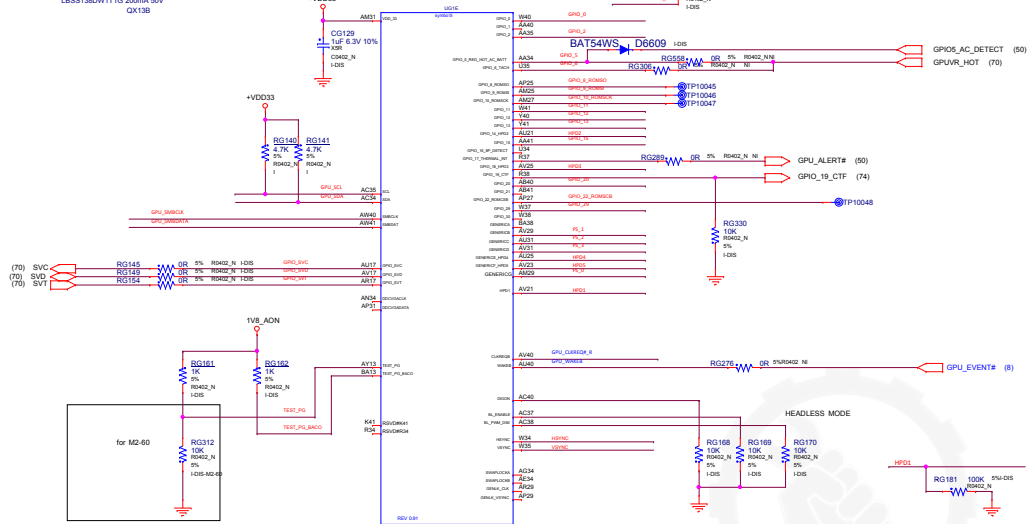


COMPONENTS SHOWN ARE EXAMPLES ONLY AND ARE NOT NECESSARILY QUALIFIED

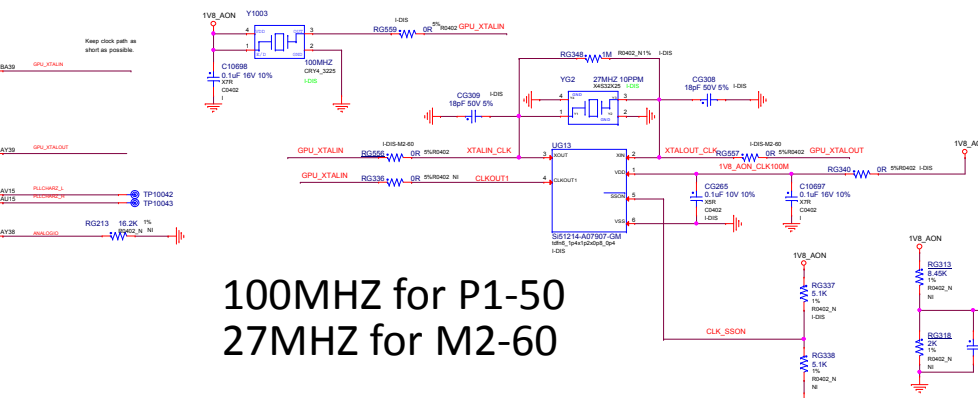
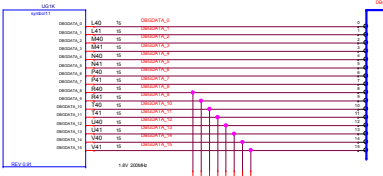
(15) ASIC GPIO Straps CLK



SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



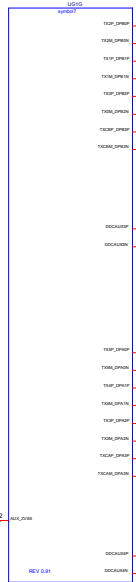
PIN STRAPS



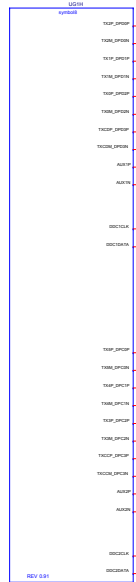
100MHZ for P1-50
27MHZ for M2-60

Project: 330S-KBL Series	
Engineer: Luffy	
Size: Title: GPU GPIO/STRAP	Rev: V01
Author: Webpage, September 27, 2011	Sheet: 78 of 81

ASIC - TMDP (A/B)



ASIC - TMDP (C/D)



ASIC - TMDP (E)

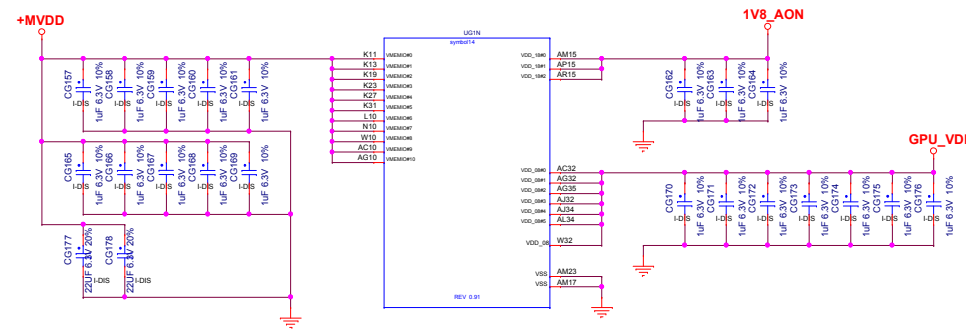
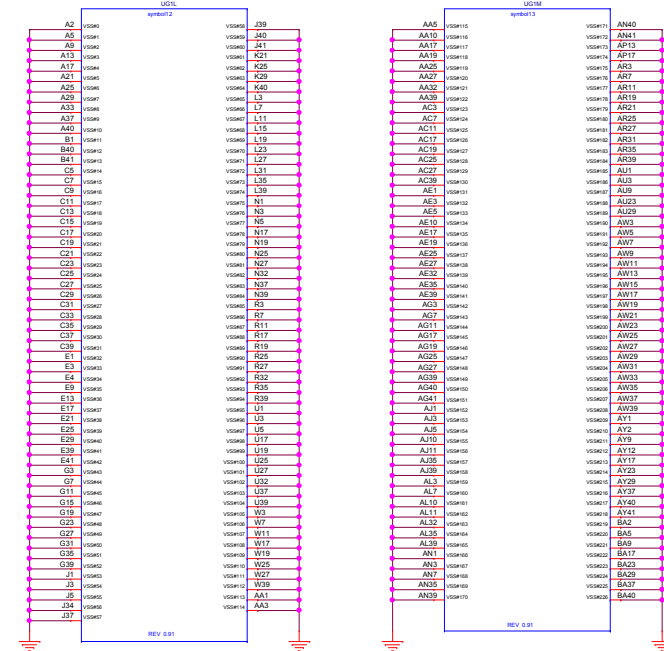
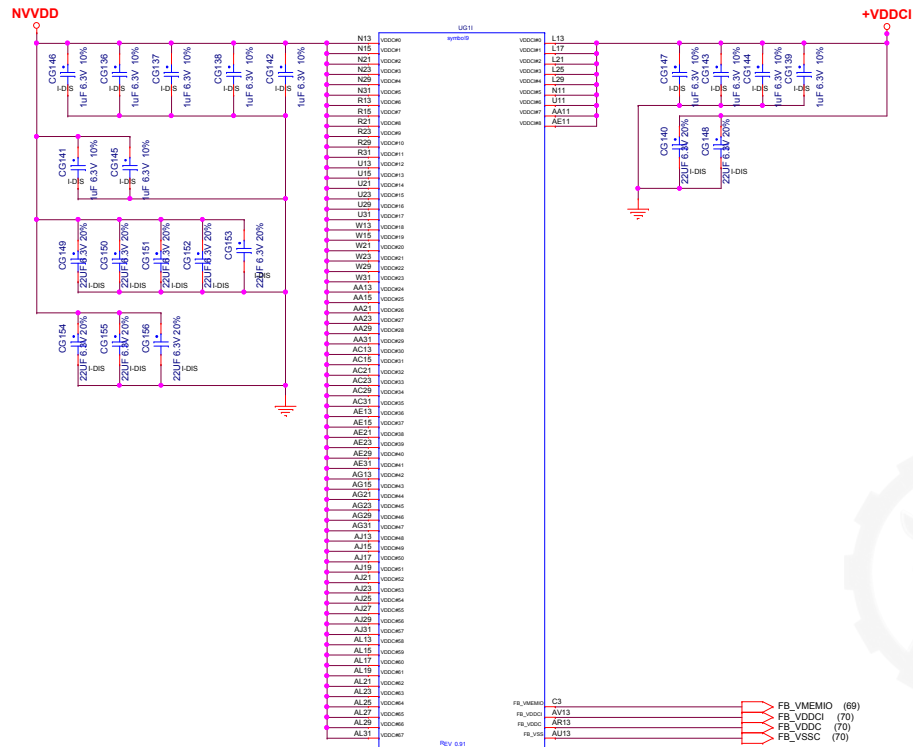


Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title	Rev	
Custom	GPU DISPLAY INTERFACE	1/01	
Date:	Tuesday, September 26, 2017	Sheet	77 of 81

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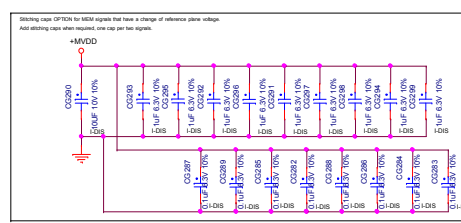
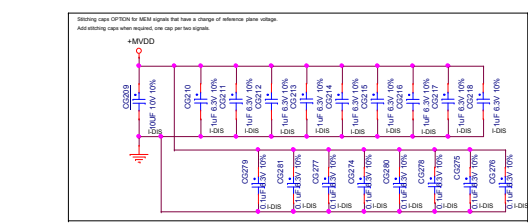
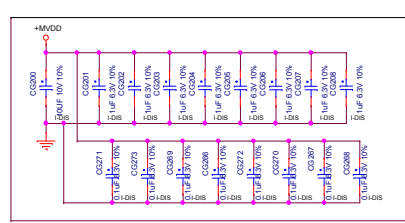
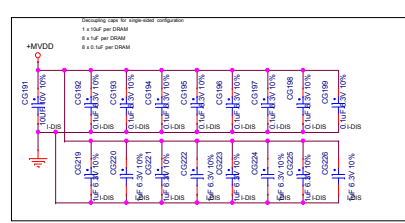
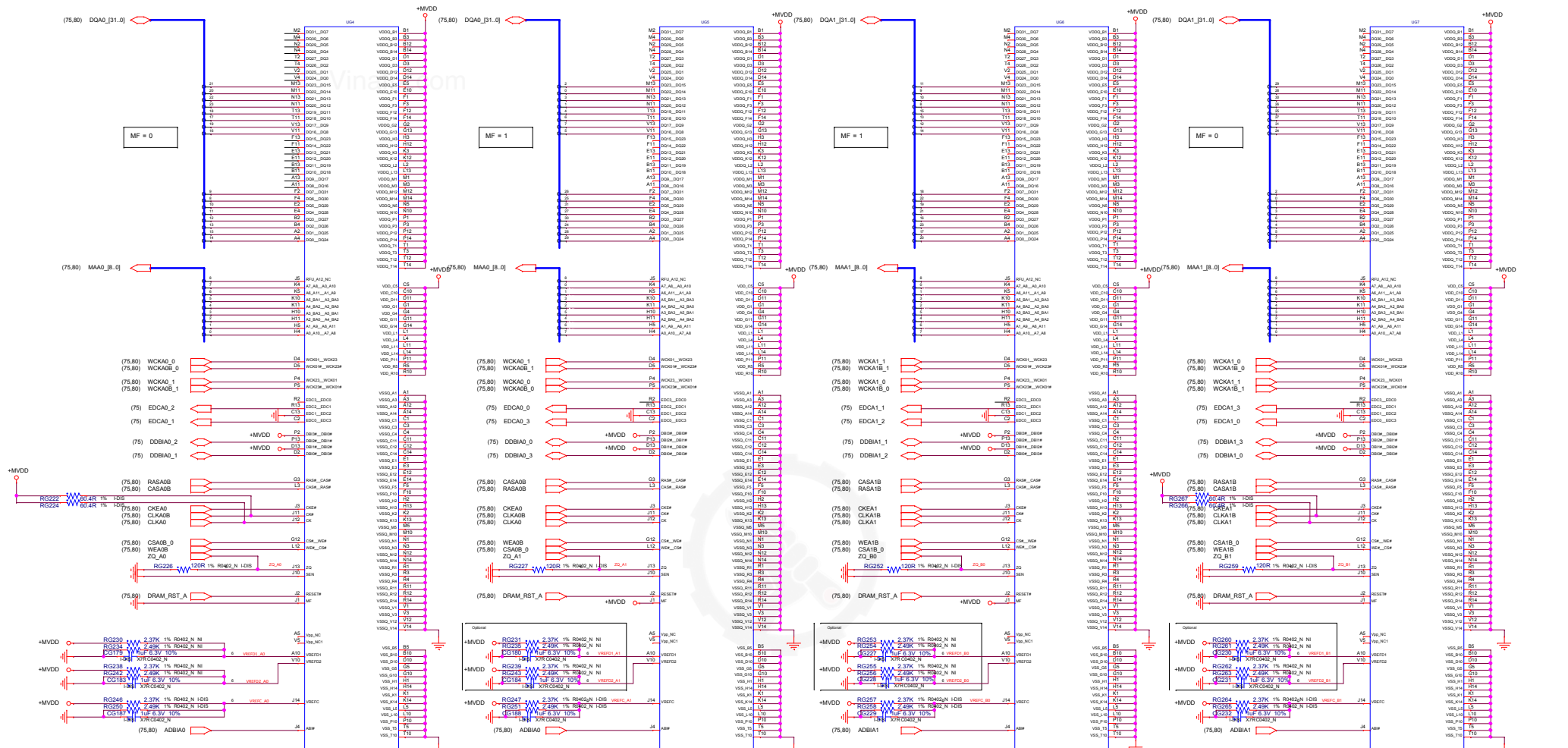
Project: 330S-KBL Series		
Engineer: Luffy		
Size	Title: NV N17S(5/5) MEM	Rev
C		V01
Date:	Tuesday, September 26, 2017	Sheet 78 of 81



For cost effective designs where VDDCI and VDD_08 are supplied by one regulator, have the VDDCI and VDD_08 balls joined on a unified power plane.

Project:		330S-KBL Series	
Engineer:		Luffy	
Size	Title: GPU POWER/GND		Rev
C			V01
Date:	Tuesday, September 26, 2017	Sheet	79 of 81

AND ARE NOT NECESSARILY QUALIFIED



Project: 330S-KBL Series	
Engineer: Luffy	
Title: VRAM (GDDR5)	Rev: V01
Date: Tuesday, September 26, 2017	Sheet: 80 of 81

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Project: 330S-KBL Series	
Engineer: Luffy	
Size: D	Rev: 001
Title: RSVVD	
Date: January 26, 2017	
Sheet: 01 of 01	