

# COMPAL CONFIDENTIAL

Eletro-XTechnical

MODEL NAME : FDI55,  
PCB NO : DA600273000  
BOM P/N : 431AII31L51

# ICL-U+MEC1418

@ : Un-pop Component  
N3@/V3@: : Inspiron (fTPM)/Vostro (HW TPM)  
ICL@/ : ICL-U  
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7  
EC@ : EC Support  
JP@/PJP@ : JUMP  
100@/1000@: Lan  
NOI2CTCH@/I2CTCH@: USB touch /I2C touch  
EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
KBBL@ : KB Backlight

750\_CTPM@:750 and china TPM  
ST\_CTPM@:ST and china TPM  
CTPM@:China TPM  
FFS@ : Free Fall Sensor  
TYPEC@ : TypeC  
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component  
PCB@/PCB\_R1@/PCB\_R3\_G@/PCB\_R3\_T@/PCB\_R3\_H@/PCB\_R3\_TM@: PC

**2019 -07 -31**  
**REV: 1.0 (A00)**



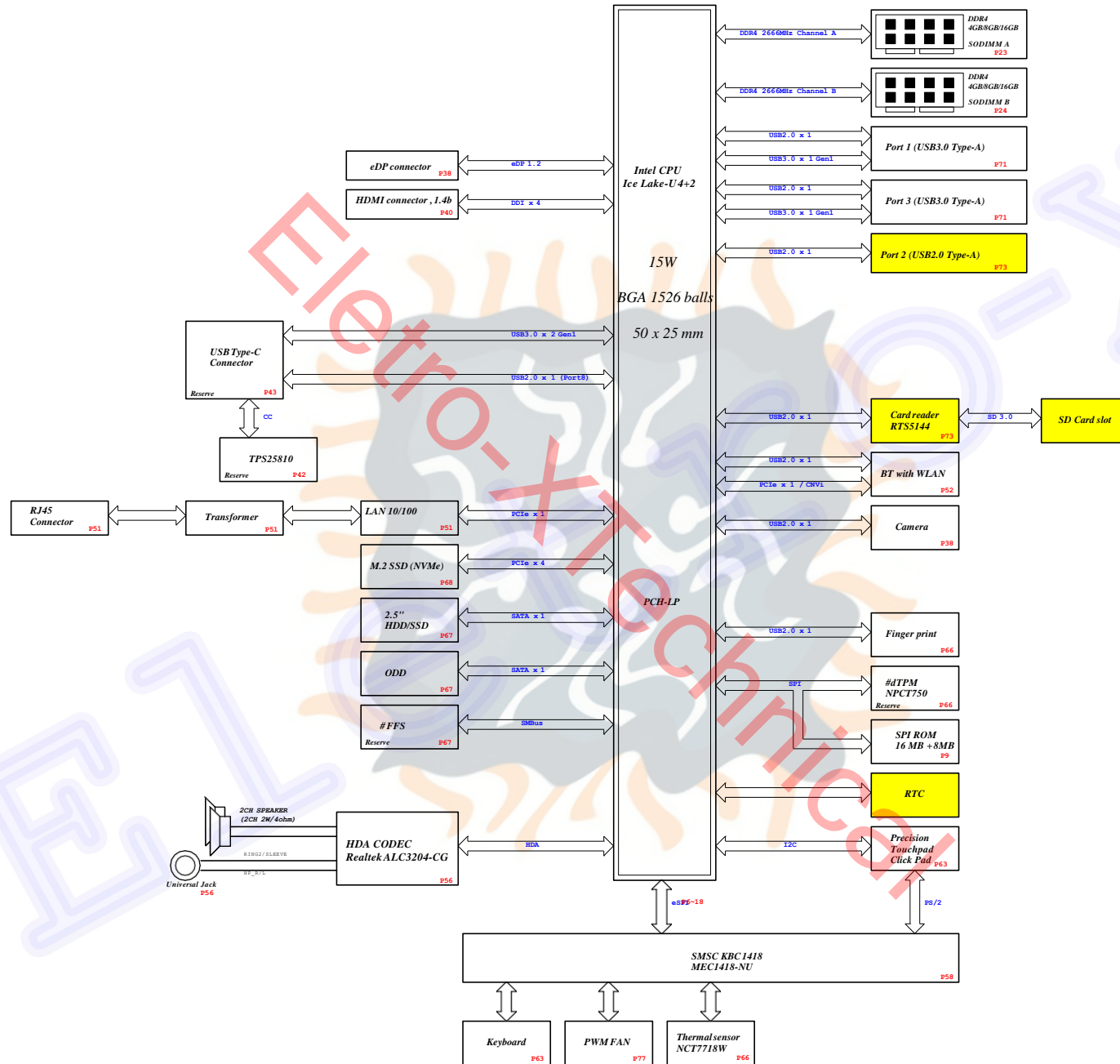
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**Eletro-X**

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Date: Wednesday, July 31, 2019				Date: Wednesday, July 31, 2019	



# Block Diagram

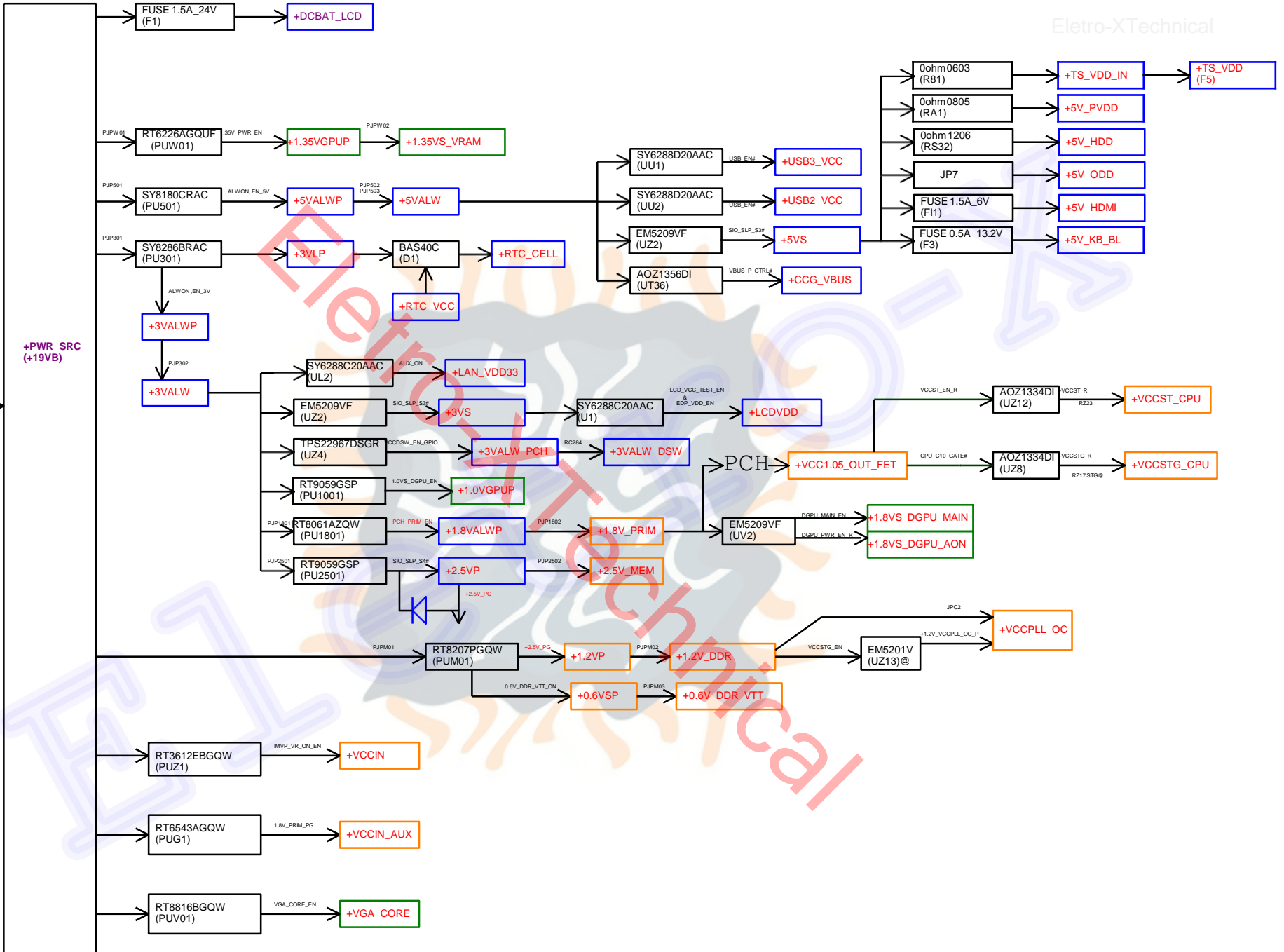
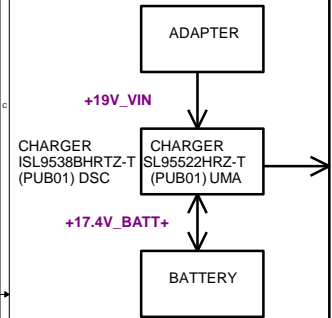


Battery	RTC
Charger	Daughter board

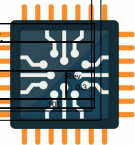
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Revision Date	20180801	Dissemination Date	20180801	Block Diagram
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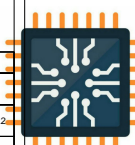
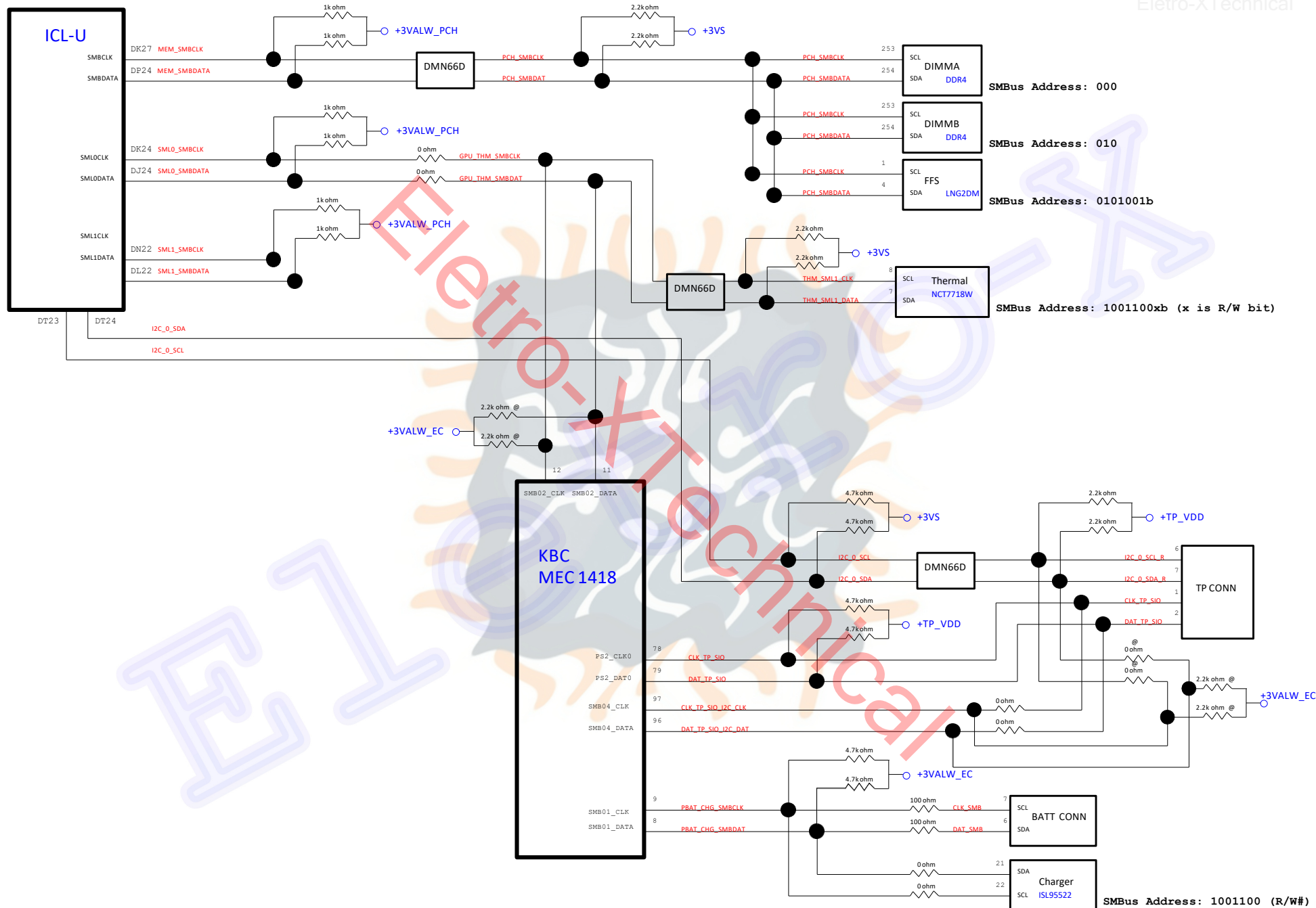


Adapter/Battery/19V  
CPU PWR  
GPU PWR  
Peripheral Device PWR



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			LA-J091P





**POWER STATES**

State	Signal	SLP_S#1	SLP_S#4	SLP_S#5	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	ON	OFF	OFF	OFF
G3		OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3		---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	Touch screen
5	Finger printer
6	CCD
7	Card reader , IO/B
8	TypeC
9	Reserved
10	BT

**Board ID & Model ID Table**

		N3V3_MLK-CML PCBA (EC-A ver)		N3V3_MLK-ICL PCBA (EC-B ver - ISL9522 / EC-C ver - ISL9536 + CGG5C)	
		Model_ID (RE4 PD-100K)	Board_ID (RE2 PD-100K)	Model_ID (RE4 PD-100K)	Board_ID (RE2 PD-100K)
SBDR (N3/V3)	UMA+N/A	RE3 PU-10K		RE3 PU-10K	
	UMA+TypeC (Data Only)	RE3 PU-17.8K	RE1 PU-10K-EVT	RE3 PU-17.8K	RE1 PU-10K-EVT
NBDR (N5/V5)	UMA+N/A	RE3 PU-27.0K	RE1 PU-17.8K-DVT1	RE3 PU-27.0K	RE1 PU-17.8K-DVT1
	UMA+TypeC (Data Only)	RE3 PU-37.4K	RE1 PU-27.0K-Reserve	RE3 PU-37.4K	RE1 PU-27.0K-Reserve
SBDR (N3/V3)	DSC+N/A	RE3 PU-49.9K	RE1 PU-37.4K-DVT2	RE3 PU-49.9K	RE1 PU-37.4K-DVT2
	DSC+TypeC (Data Only)	RE3 PU-64.9K	RE1 PU-49.9K-Reserve	RE3 PU-64.9K	RE1 PU-49.9K-Reserve
NBDR (N5/V5)	DSC+N/A	RE3 PU-82.5K	RE1 PU-64.9K-Pilot	RE3 PU-82.5K	RE1 PU-64.9K-Pilot
	DSC+TypeC (Data Only)	RE3 PU-107K	RE1 PU-82.5K-Reserve	RE3 PU-107K	RE1 PU-82.5K-Reserve

**Voltage Rails**

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6V5 power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+1.35V_MEM_GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VG5	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VG5	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

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 副寄: Chen, AlexCL (TPE); Chang, Gary J; Hoias, Jimmy  
 主题: RE: ICL N3V3 MLK High Power Consumption on VCCIN\_AUX Under S3/S5

Hi David,  
 VCCIN\_AUX only down to 0V while SLP\_S0# is asserted.  
 On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,  
 Eddie Wu +886-2-66221110

**Table 11-23. System with M3 State Supported**

Rails	SKUs	S0/M0 <sup>3</sup>	C10 <sup>2</sup>	S0ix/M-off <sup>4</sup>	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3 <sup>1</sup>
RTC Well	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
3.3V_DSW	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.8A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VNN_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V1.05_BYPASS	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
V1.8M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
VCCST <sup>12, 15</sup>	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	ON	OFF <sup>5</sup>	OFF	No Power
VCCSTG	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
TCSS/AGSH	All	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	ON	ON	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL_OC <sup>12</sup>	All	ON	ON	OFF <sup>11</sup>	ON <sup>8, 13</sup>	ON <sup>8, 13</sup>	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON <sup>11</sup>	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON <sup>11</sup>	ON	OFF <sup>14</sup>	ON	OFF <sup>14</sup>	OFF	No Power

Note : VCCIN\_AUX only down to 0V while SLP\_S0# is asserted. On S3 mode, it only can down to 1.1V.

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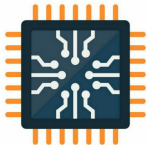
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USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		USB3.0 (Type-C)
USB3.0-4	PCIE-4		USB3.0 (Type-C)
USB3.0-5	PCIE-5		GPU
USB3.0-6	PCIE-6		GPU
	PCIE-7		GPU
	PCIE-8		GPU
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA HDD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

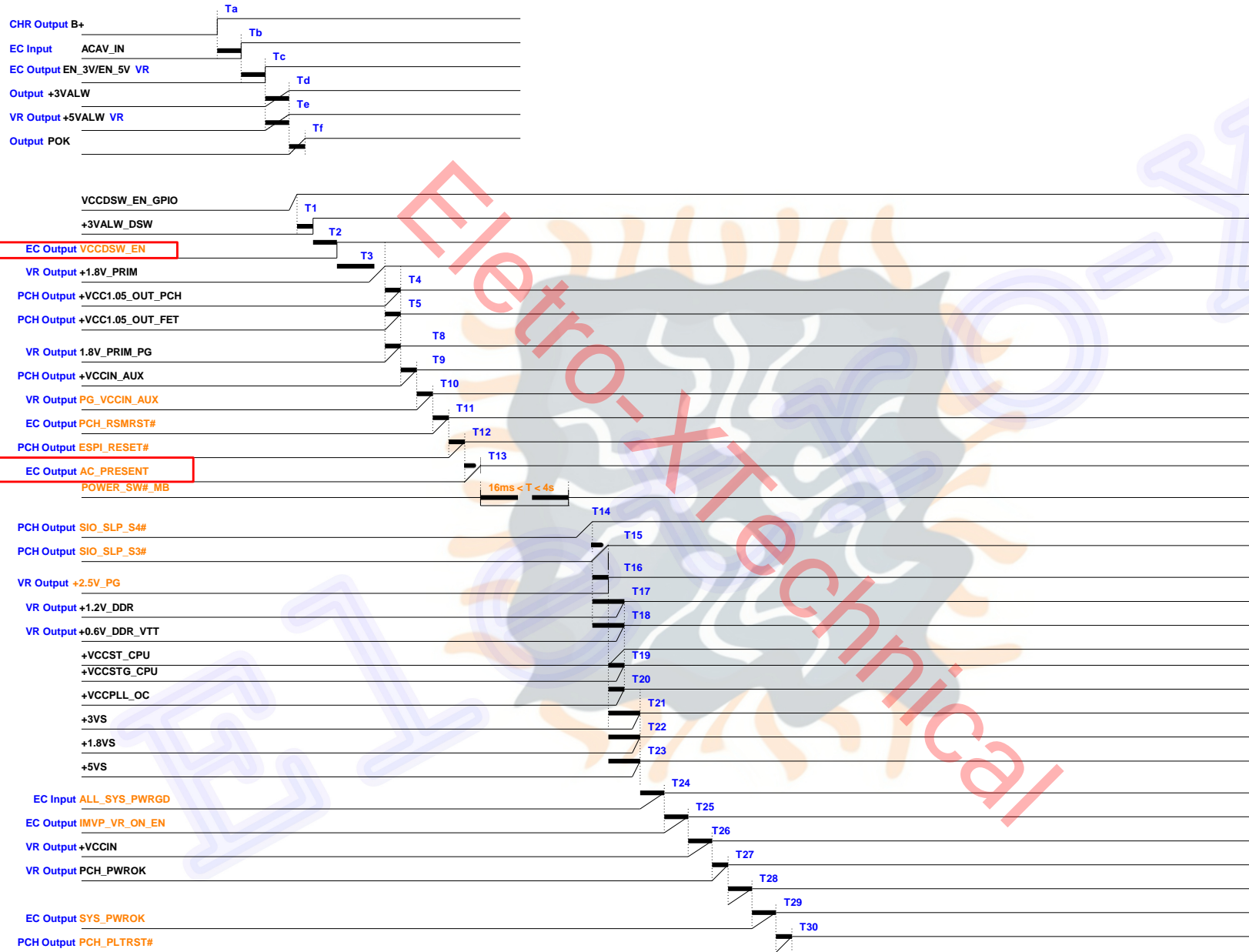
**High Speed I/O (HSIO) Lane Multiplexing in ICL U PCH-LP**



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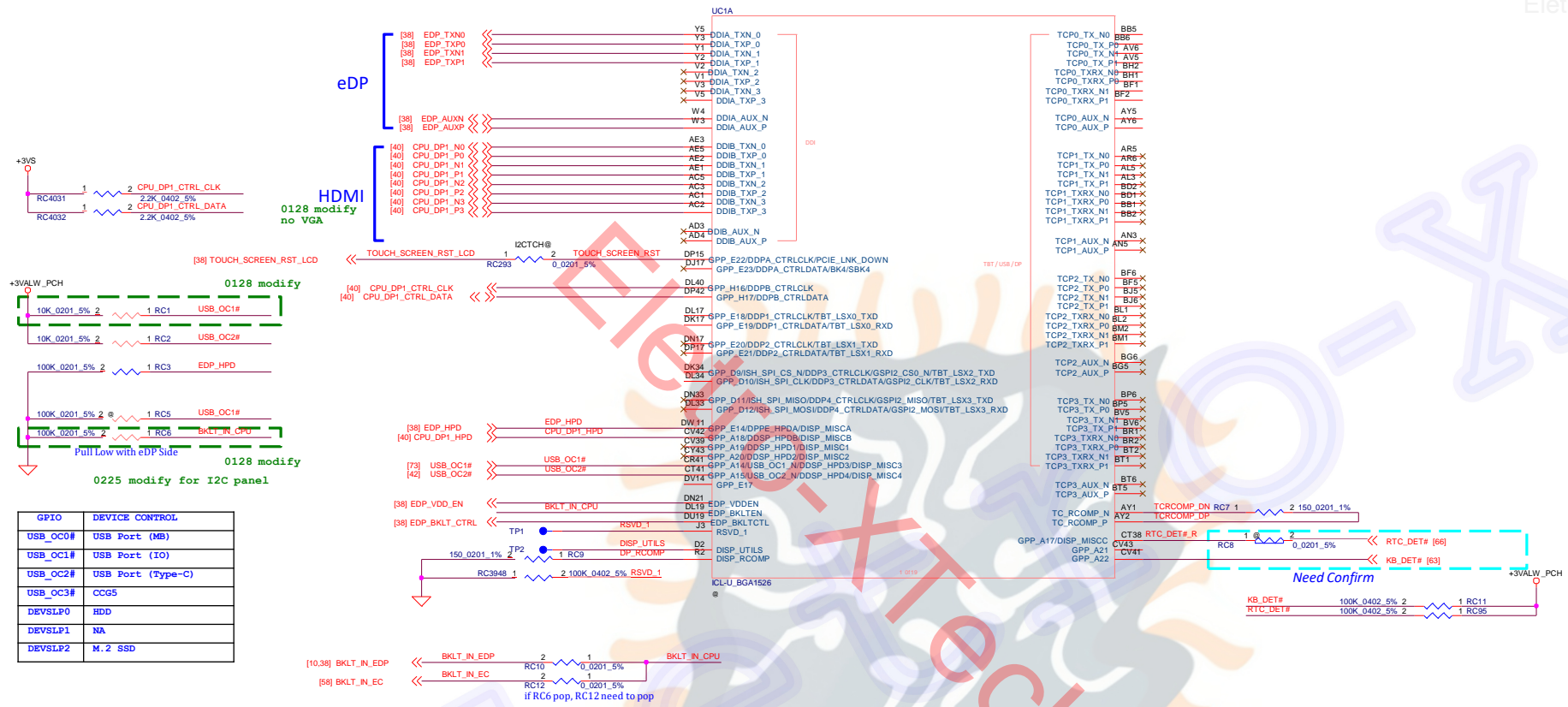


# Power Up Sequence



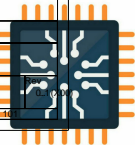
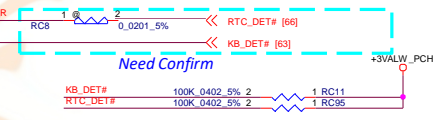
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			Size/Document Number LA-J091P
			Rev 0.2
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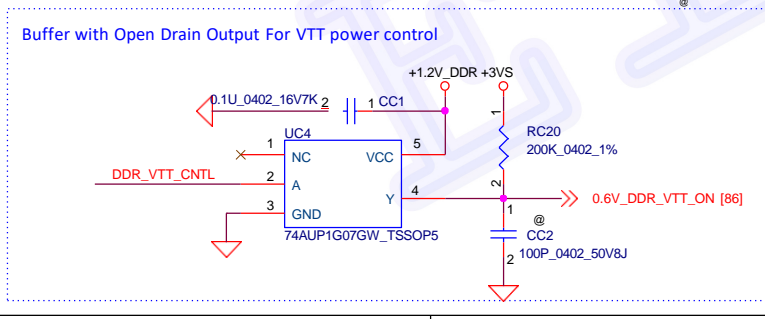
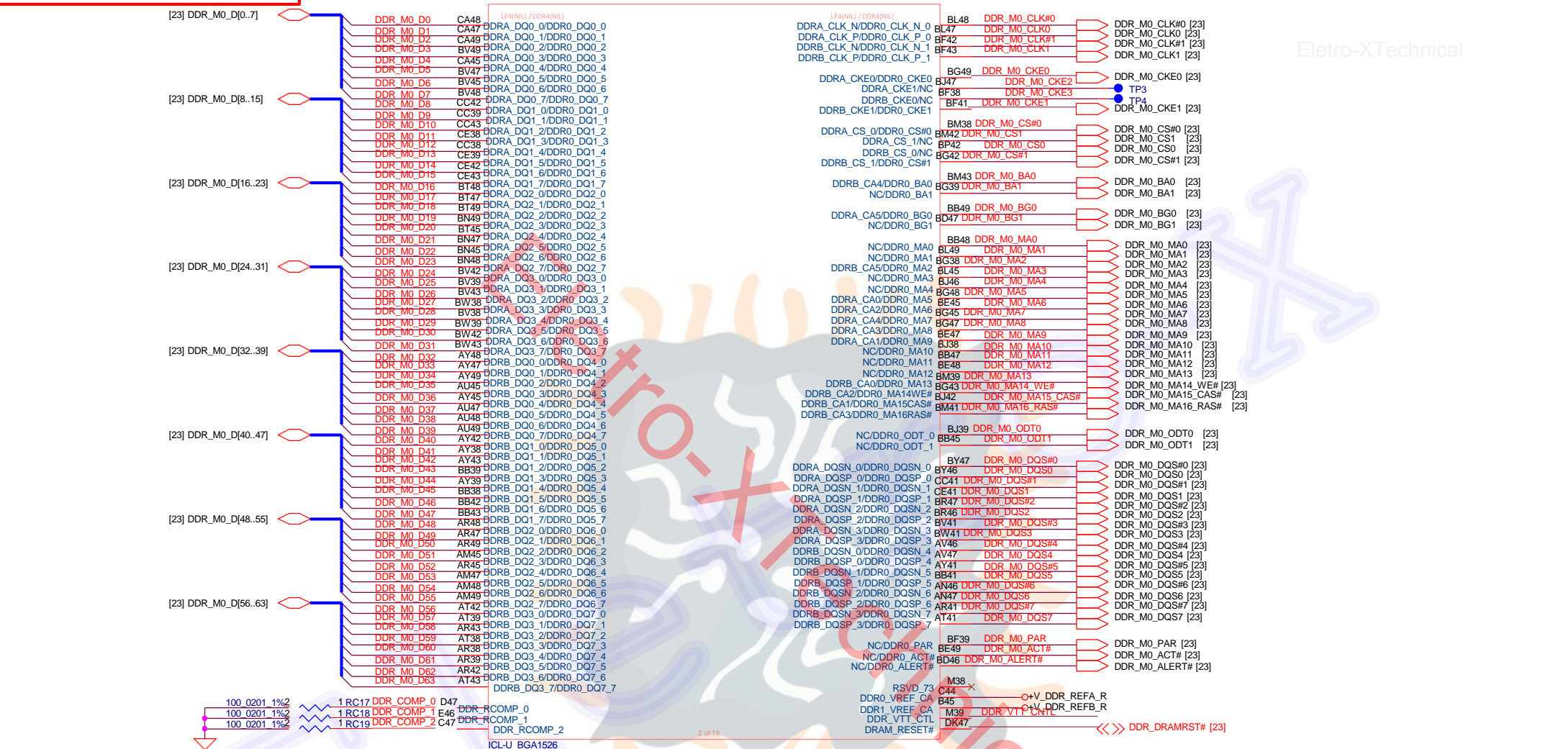


GPIO	DEVICE CONTROL
USB_OC0#	USB Port (MB)
USB_OC1#	USB Port (IO)
USB_OC2#	USB Port (Type-C)
USB_OC3#	CCG5
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD

[10,38] BKLT\_IN\_EDP << BKLT\_IN\_EDP RC10 2 0.0201\_5%  
 [58] BKLT\_IN\_EC << BKLT\_IN\_EC RC12 2 0.0201\_5%  
 if RC6 pop, RC12 need to pop

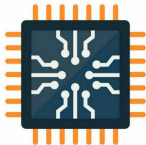


**Main Function: CPU (2/13)**



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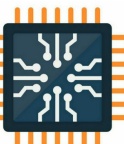
Note: trace width=20 mils, spacing of adjacent signal=20 mils







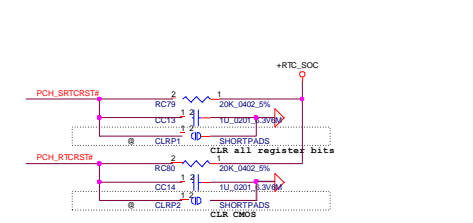
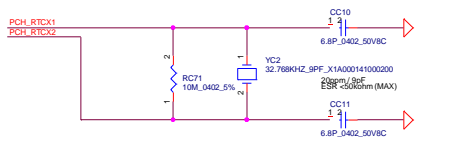
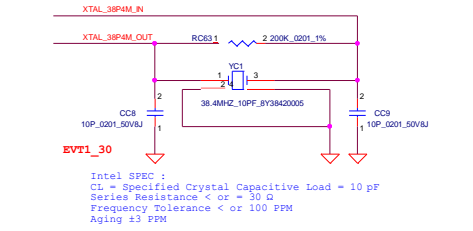
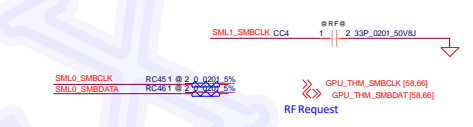
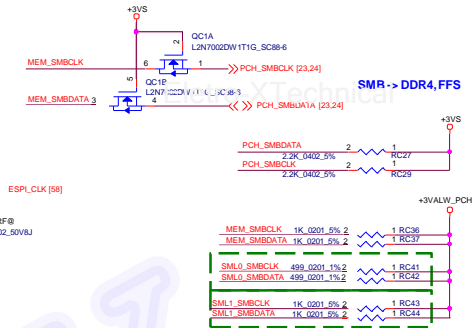
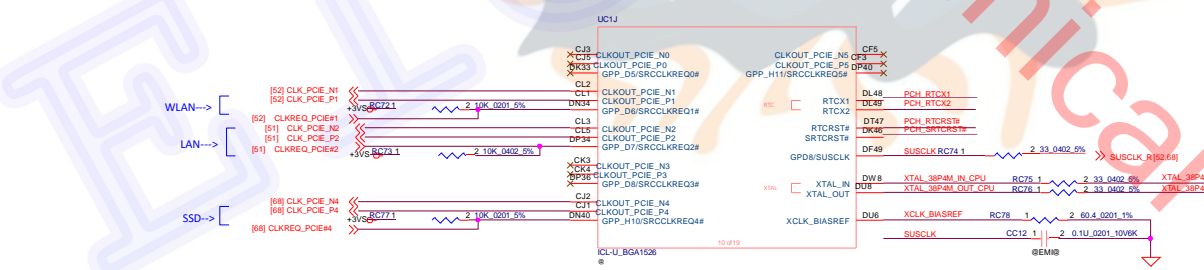
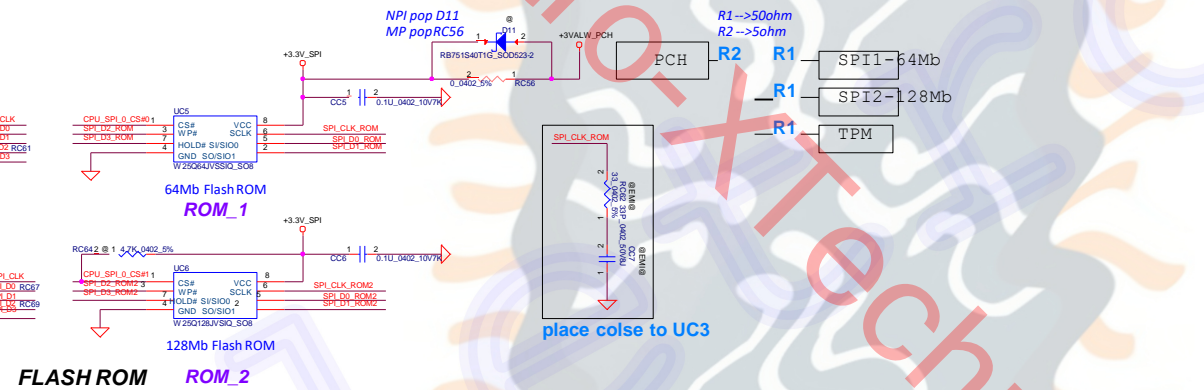
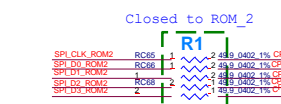
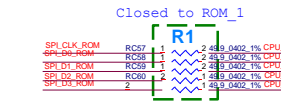
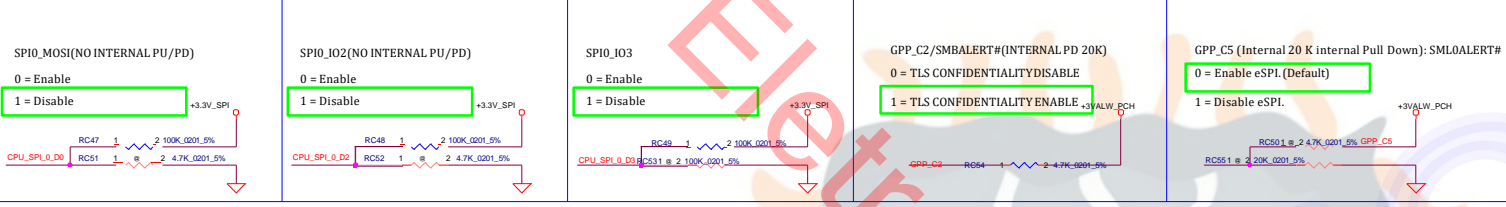
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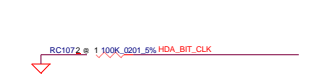
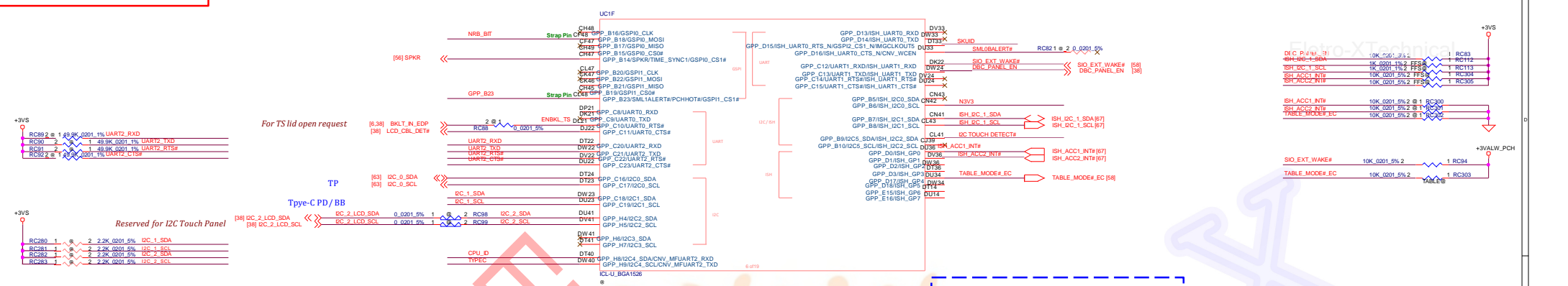
**Main Function: CPU (4/13)**

RC22 @ 4.99_0402_1% SD034496980	RC22 S RES 1/16W 0+5% 0402 SD029000080
RC23 @ 4.99_0402_1% SD034496980	RC23 S RES 1/16W 0+5% 0402 SD029000080
RC24 @ 4.99_0402_1% SD034496980	RC24 S RES 1/16W 0+5% 0402 SD029000080
RC25 @ 4.99_0402_1% SD034496980	RC25 S RES 1/16W 0+5% 0402 SD029000080
RC26 @ 4.99_0402_1% SD034496980	RC26 S RES 1/16W 0+5% 0402 SD029000080

R2 Resistor should be 50 for 1.8V and 3.3V.  
R2 to be placed on SPI0\_CLK, SPI0\_MISO, SPI0\_MOSI, SPI0\_I0\_2 and SPI0\_I0\_3. It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.



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NO REBOOT	CPUNSSC CLOCK FREQ	TOP SWAP OVERRIDE
<p>GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)</p> <p>0 = REBOOTENABLED</p> <p>1 = NO REBOOT</p>	<p>GPP_B23 (Internal 20 K Pull Down)</p> <p>0 = 38.4 MHz clock (direct from crystal) (default)</p> <p>1 = 19.2 MHz clock (from internal divider)</p>	<p>GPP_B14 / SPKR (Internal 20 K Pull Down)</p> <p>0 = Disable "Top Swap" mode. (Default)</p> <p>1 = Enable "Top Swap" mode.</p>
<p>NRB_BIT RC1141 @ 2.47K 0.001 5%</p>	<p>GPP_B23 RC1151 @ 2.47K 0.001 5%</p>	<p>SPKR RC1161 @ 2.92K 0.001 5%</p>

Pin Name	I2C TOUCH DETECT#
TPM	LOW V3@
fTPM	HIGH N3@

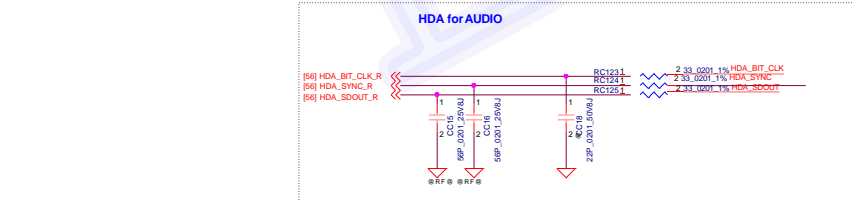
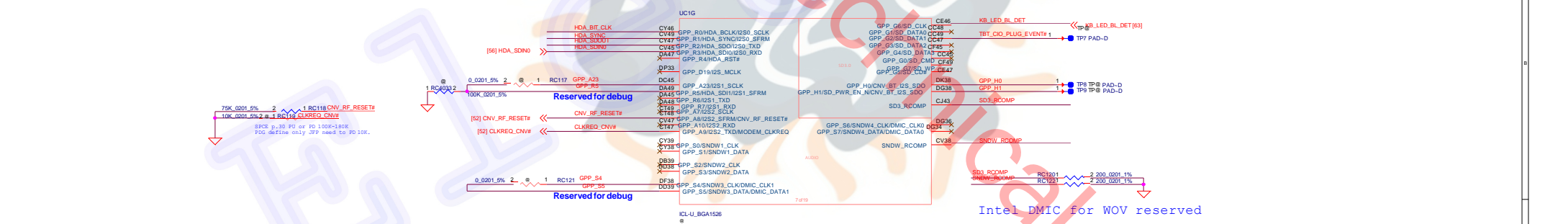
**TPM/fTPM**

Pin Name	I2C TOUCH DETECT#
I2C TOUCH	LOW I2CTCH@
USB TOUCH	HIGH NOI2CTCH@

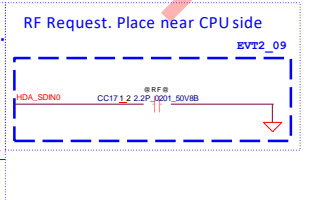
**I2C TOUCH DETECT#**

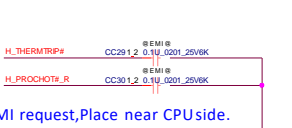
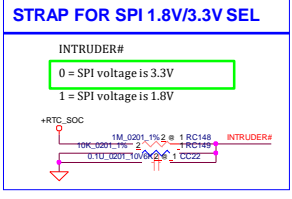
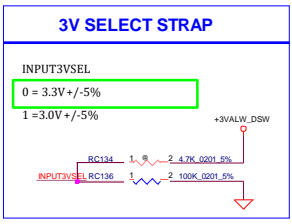
Pin Name		SKUID
LOW	UMA UMA@	
HIGH	DSC DIS@	

**Strap Pin**

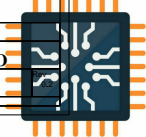
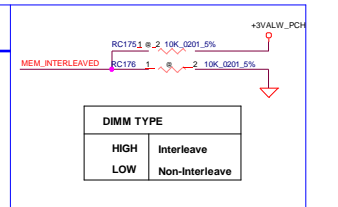
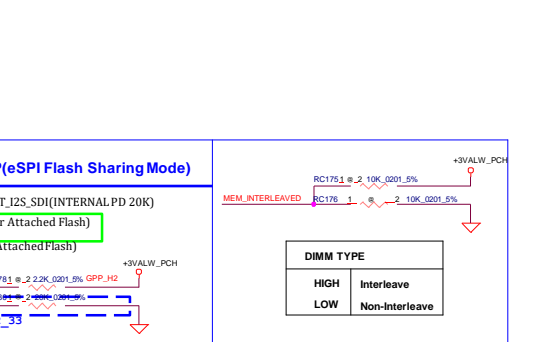
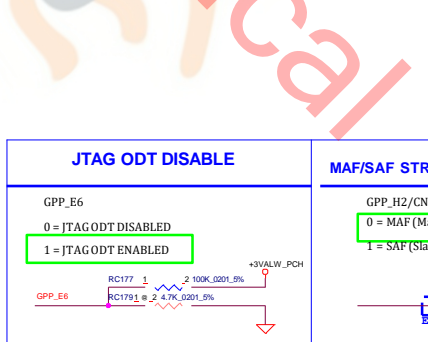
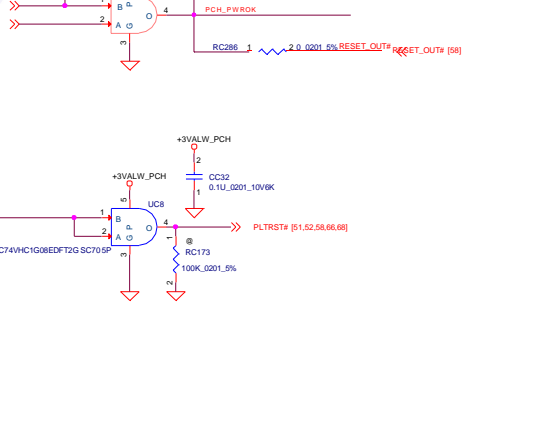
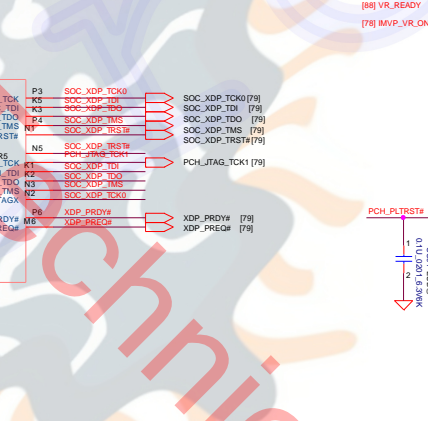
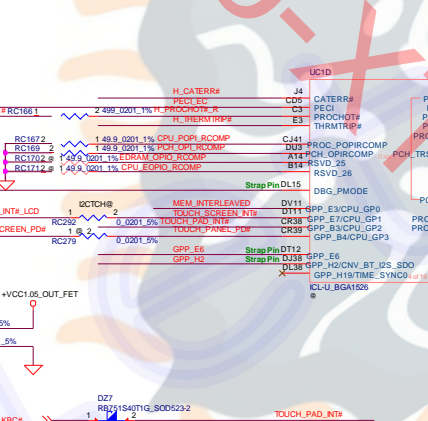
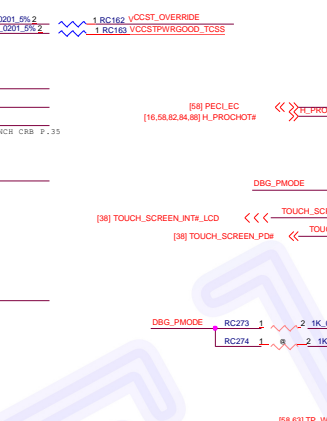
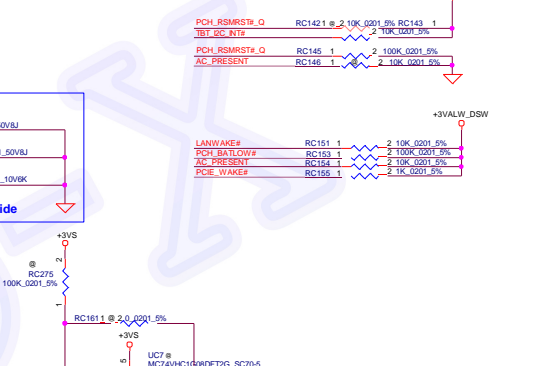
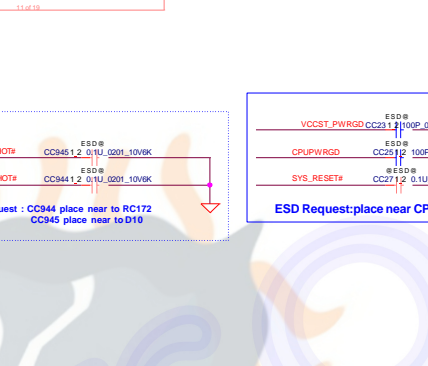
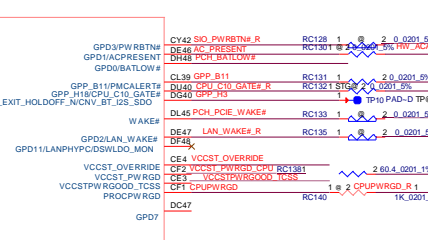
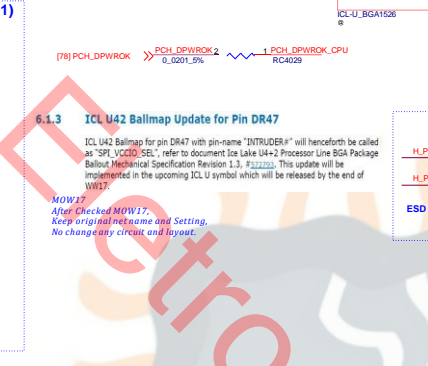
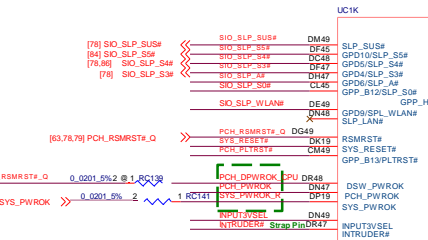
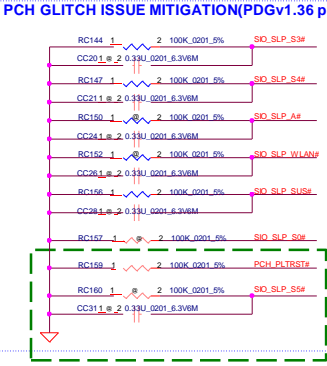
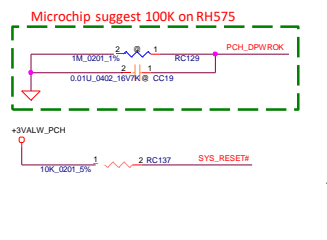
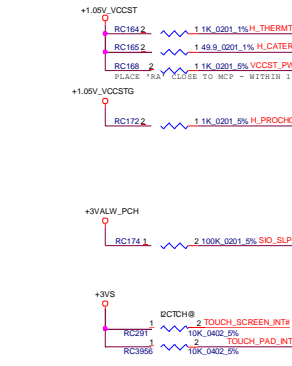


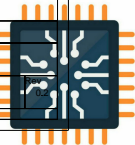
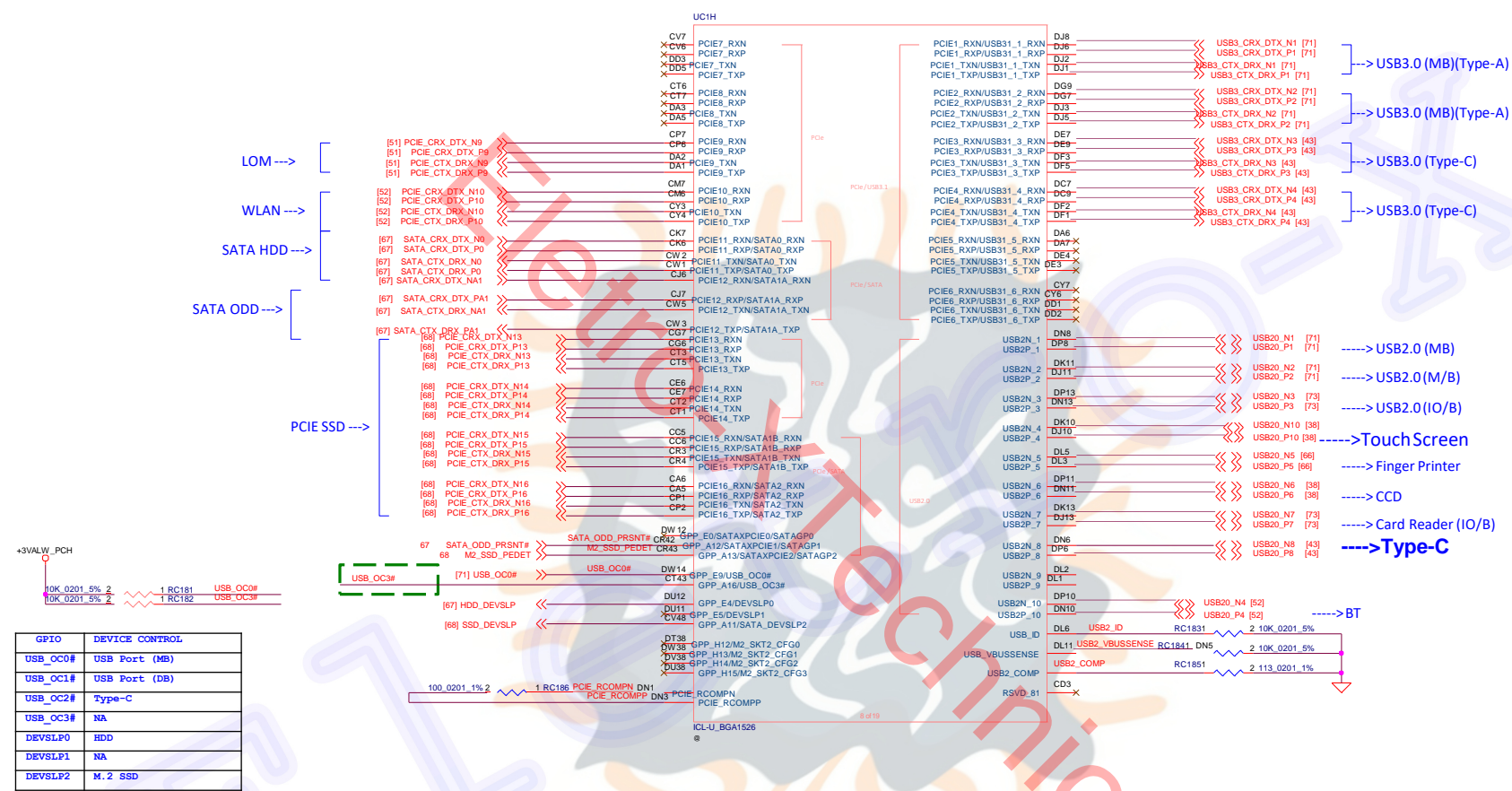
FLASH DESCRIPTOR SECURITY OVERRIDE
<p>GPP_R2/HDA_SDO (Internal 20 K Pull Down)</p> <p>0 = ENABLE (DEFAULT)</p> <p>1 = DISABLE (ME update)</p>
<p>ME_FWP_PCH RC126 @ 1K 0.001 1%</p>

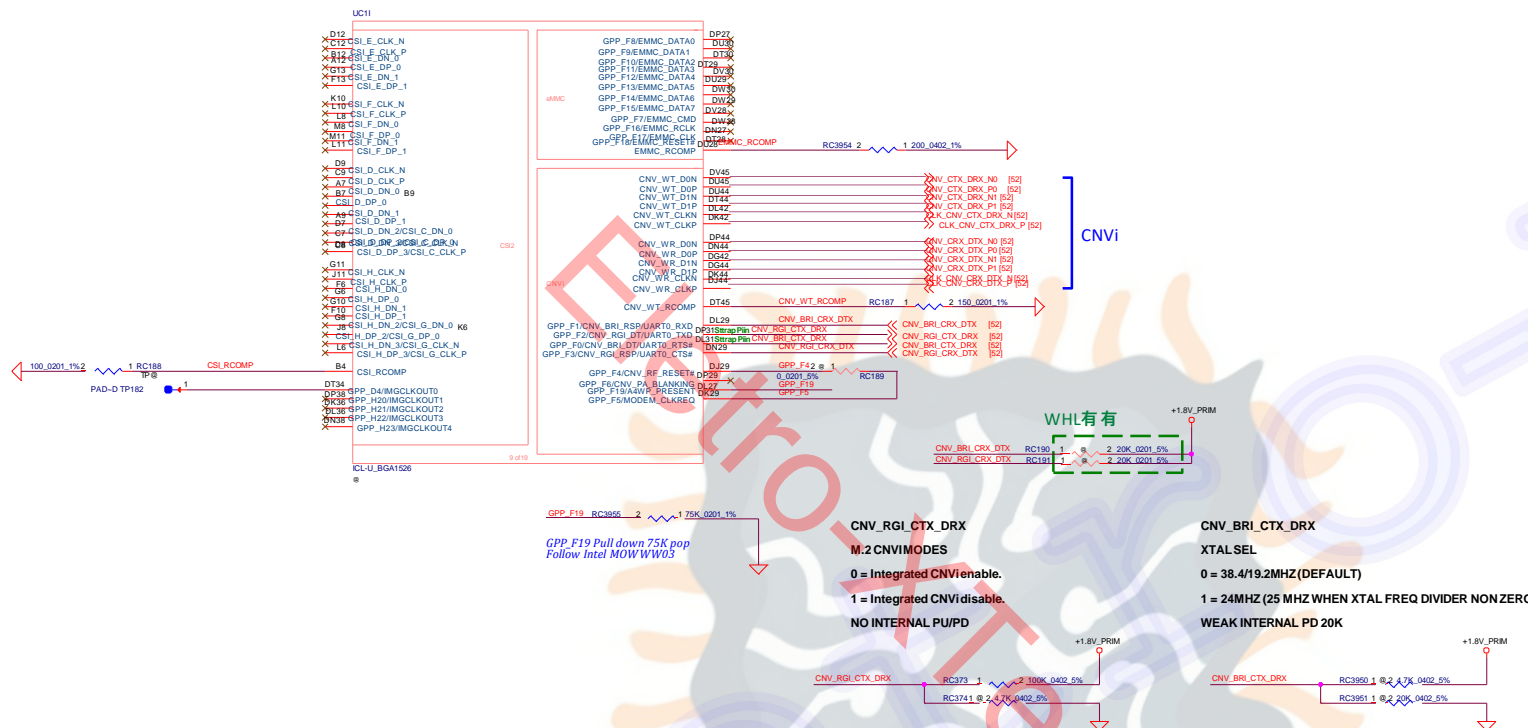




EMI request, Place near CPU side.





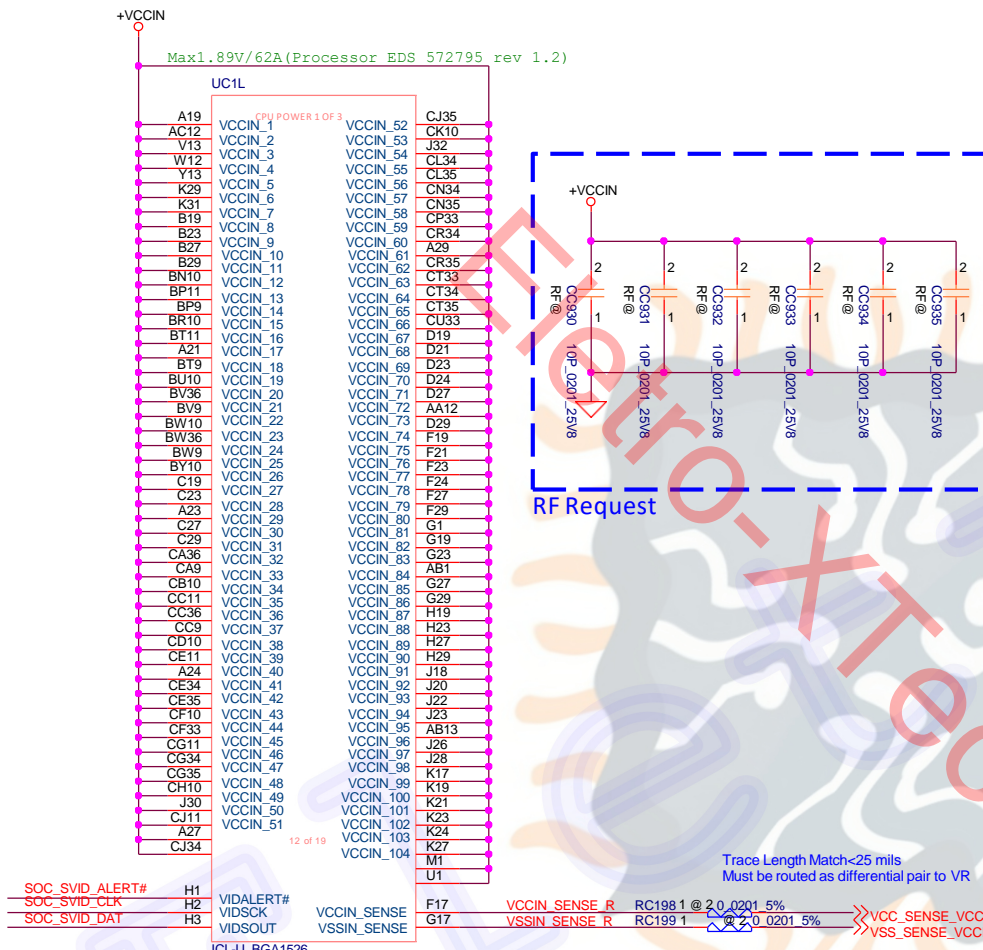


GPP\_F19 RC3955 2 120K 0.201 1%  
 GPP\_F19 Pull down 75K pop  
 Follow intel MOWWW03

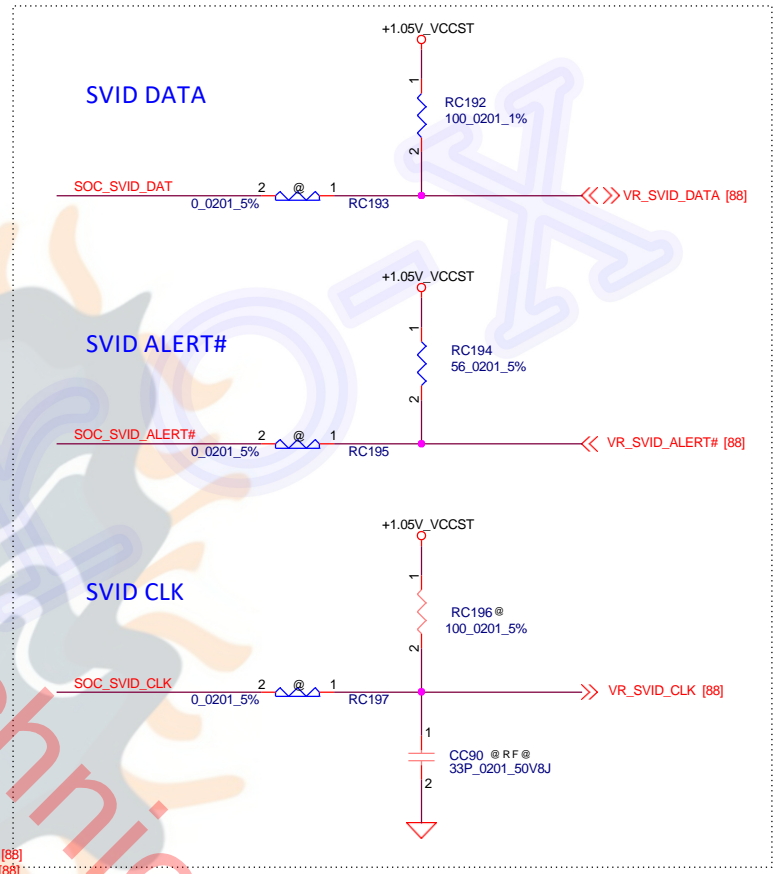
**CNV\_RGI\_CTX\_DRX**  
 M:2 CNVIMODES  
 0 = Integrated CNVenable.  
 1 = Integrated CNVIdisable.  
 NO INTERNAL PUPPD

**CNV\_BRI\_CTX\_DRX**  
 XTALSEL  
 0 = 38.4/19.2MHZ (DEFAULT)  
 1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)  
 WEAK INTERNAL PD 20K

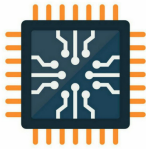


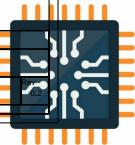
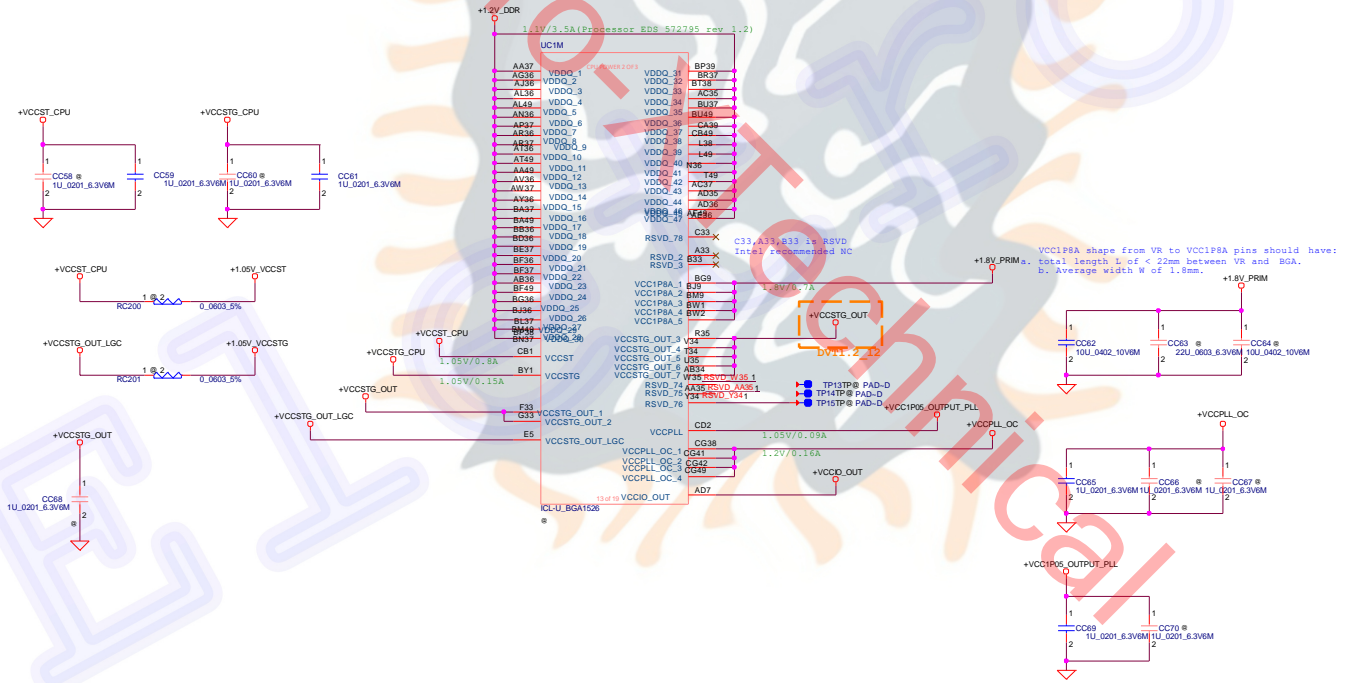
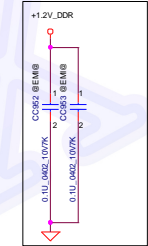
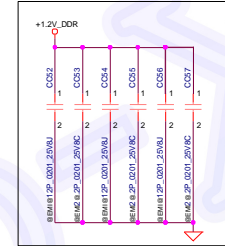
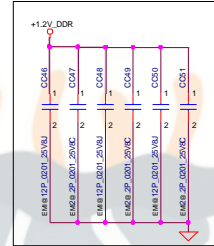
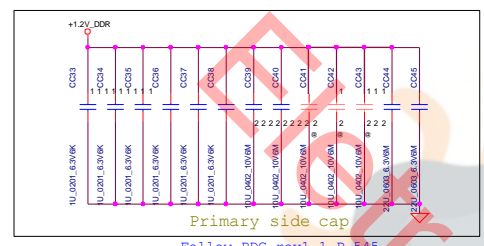


1. The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch).
  2. Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU

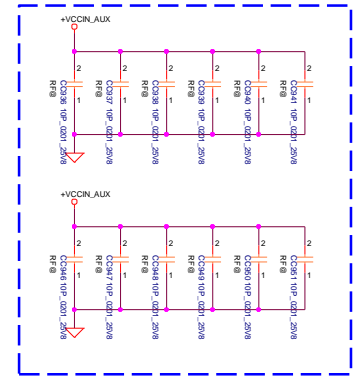


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1.8V/27 A(PCH\_BSS\_572631 rev 1.0)

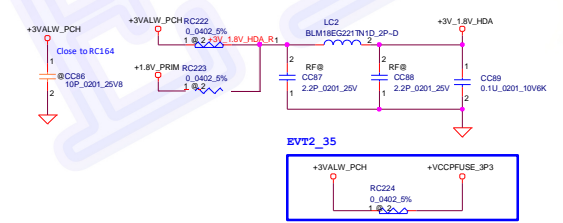
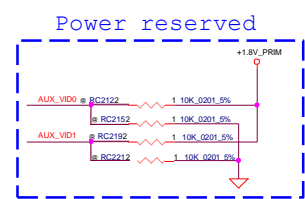
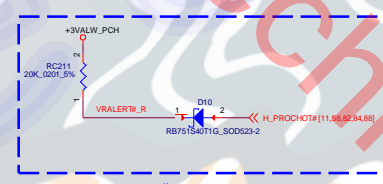
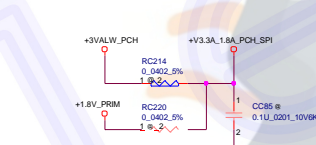
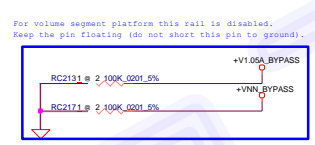
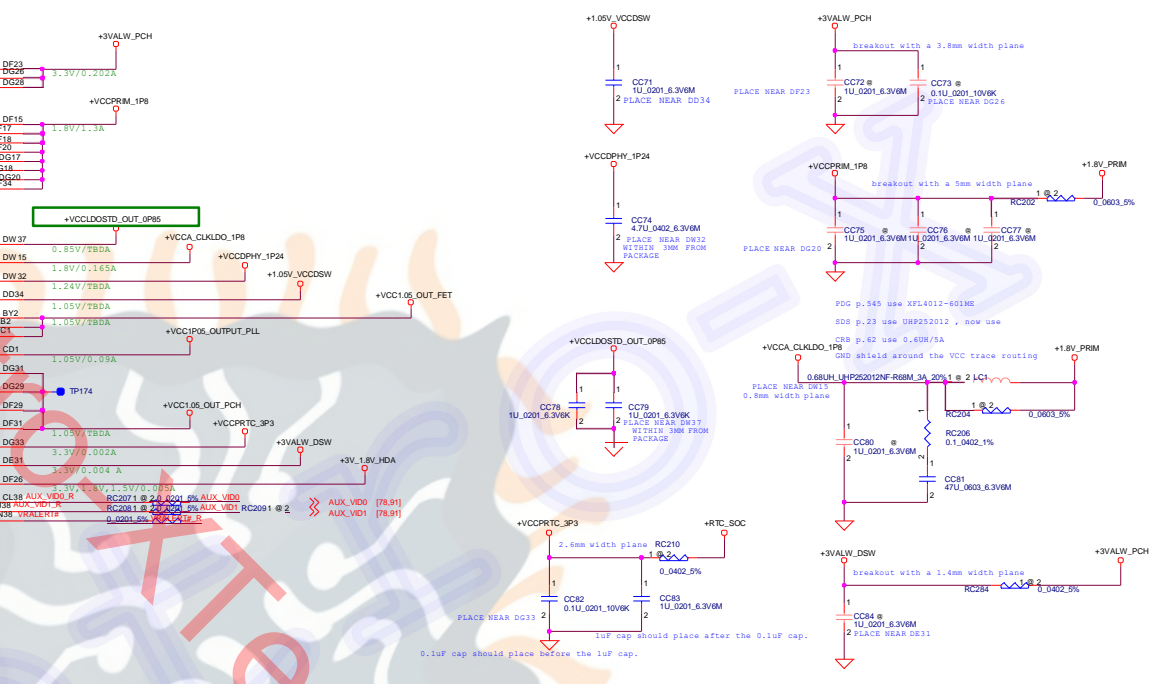
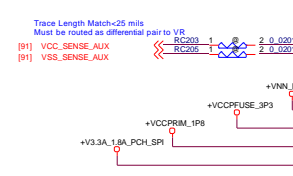
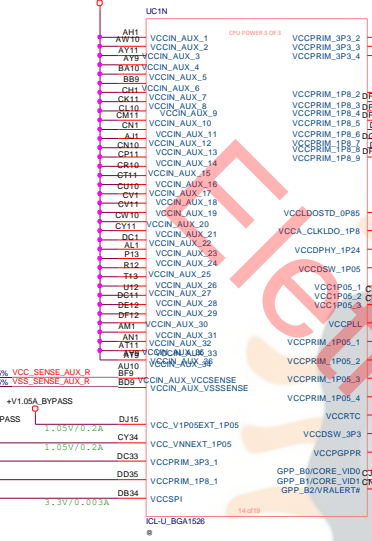


Table 11-1. VCCIN\_AUX VID

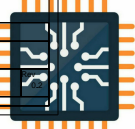
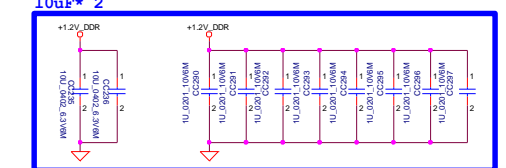
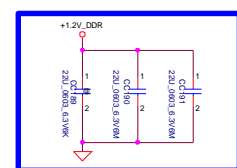
VBS(1) Pin State	VBS(5) Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.85	Full Current, 0CLV
1	1	1.8	Normal mode for 10V-0V Full-current, 0CLV

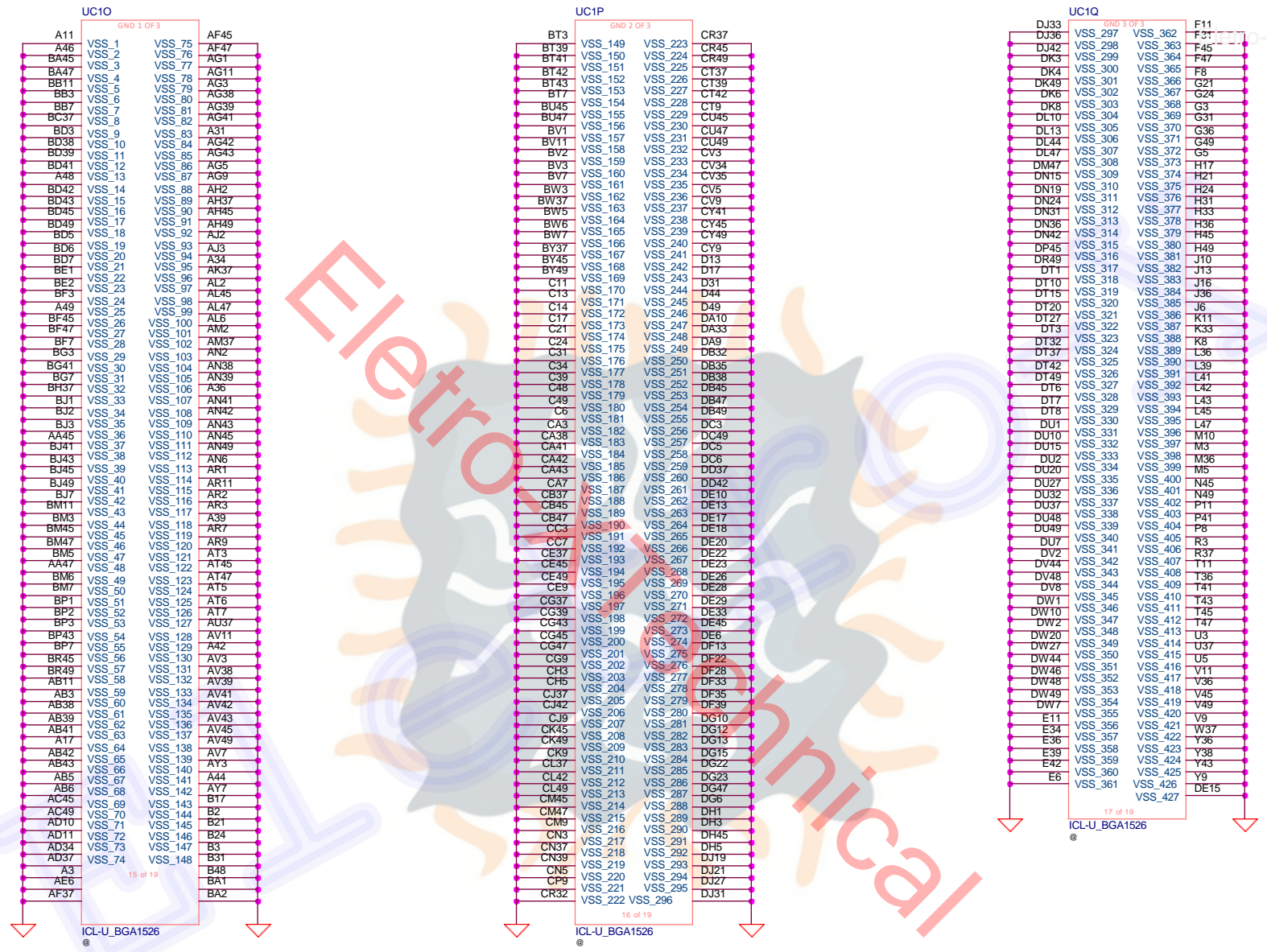
Note: Logic "0" is 0V and Logic "1" is 1.8V based logic, but the VID pins must be 3.3V tolerant as well.

Refer 575034\_ICL\_U42\_DDR4\_T3\_6L\_Core\_Schematics\_Rev0p7.pdf

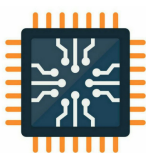
Place on CPU Side 22uF\* 2 + 22uF\* 1 (Reserved)

Place on opposite of CPU Side 1uF\* 8 10uF\* 2



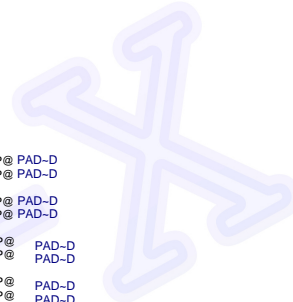
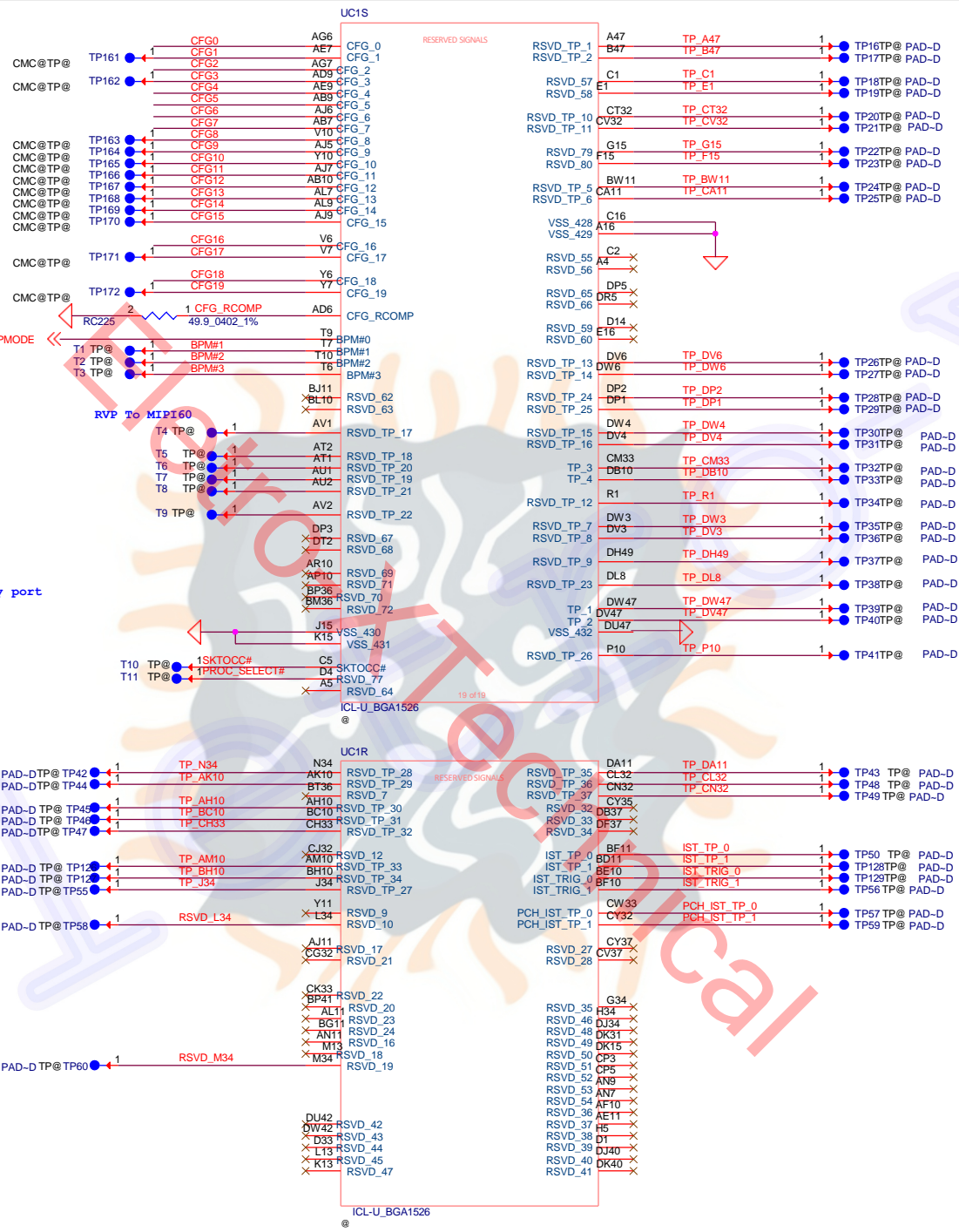
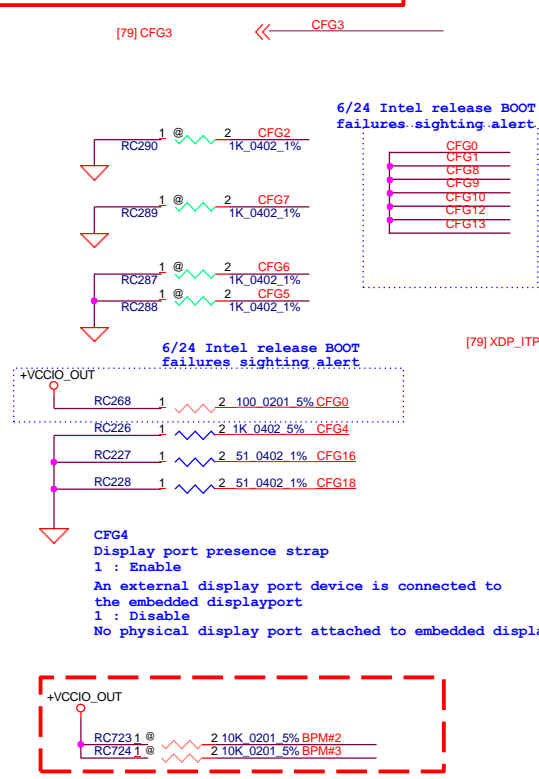


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# Main Function: CPU(13/13)

Eletr-XTechnical



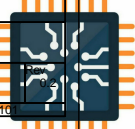
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Issued Date	2018/04/01	Deciphered Date	2019/04/01
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**Compal Electronics, Inc.**

Title: **WHL-U(12/12)RSVD**

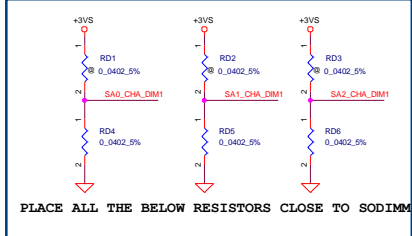
Document Number: **LA-J091P**

Date: Monday, July 23, 2019 Sheet 18 of 10



# CHANNEL-M0

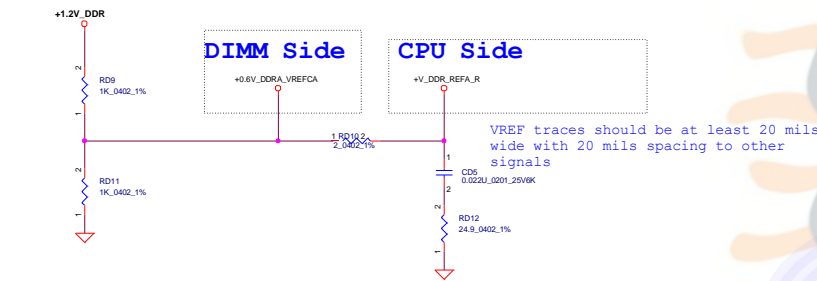
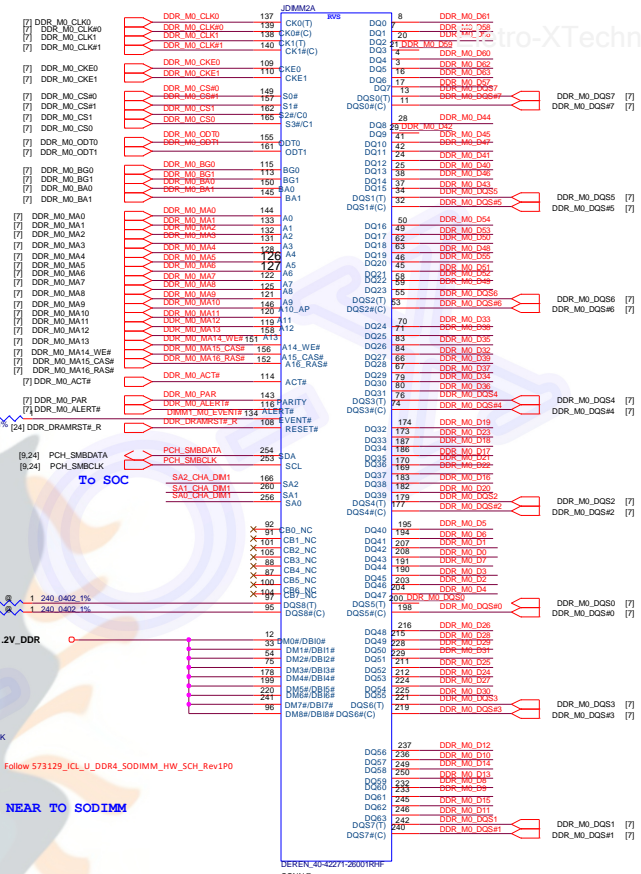
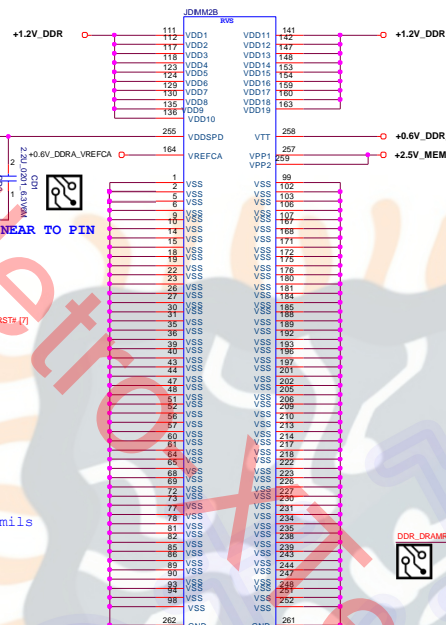
BOT: DIMM1 (JDIMM2 CONN) Non-ECC DIMM



SPD ADDRESS FOR CHANNEL A :  
SA0 = 0; SA1 = 0; SA2 = 0.

## Non-Interleaved Memory

- [7] DDR\_M0\_DQ[15]
- [7] DDR\_M0\_CS[16..31]
- [7] DDR\_M0\_CS[32..47]
- [7] DDR\_M0\_CS[48..63]



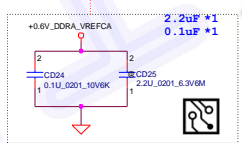
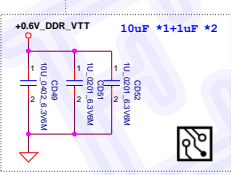
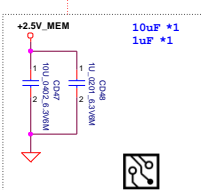
### Decoupling Cap\_Channel A

Layout Note:  
Place near JDIMM2.257,259

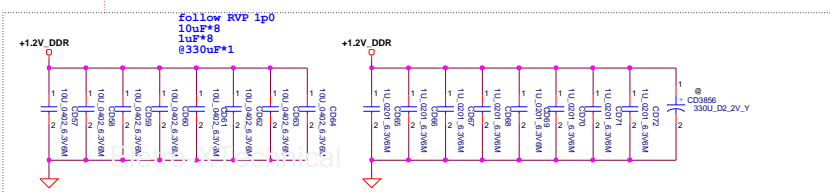
Layout Note:  
Place near JDIMM2.258

Layout Note:  
PLACE THE CAP near JDIMM2. 164

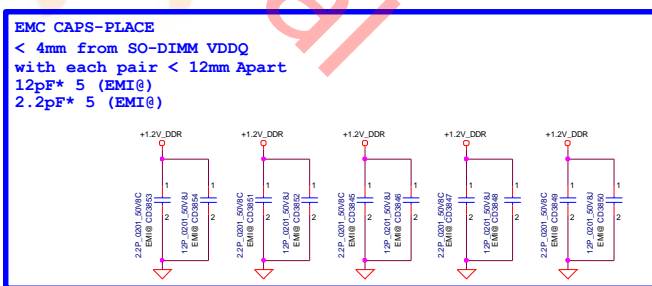
C107 place near JDIMM2



Layout Note:  
Place near JDIMM2



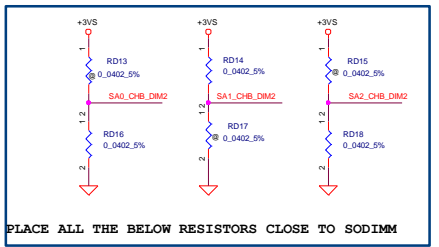
Part Number:SP07001CY0L  
Part description:S SOCKET LOTES ADDR0206-P001A02 DDR4 A31



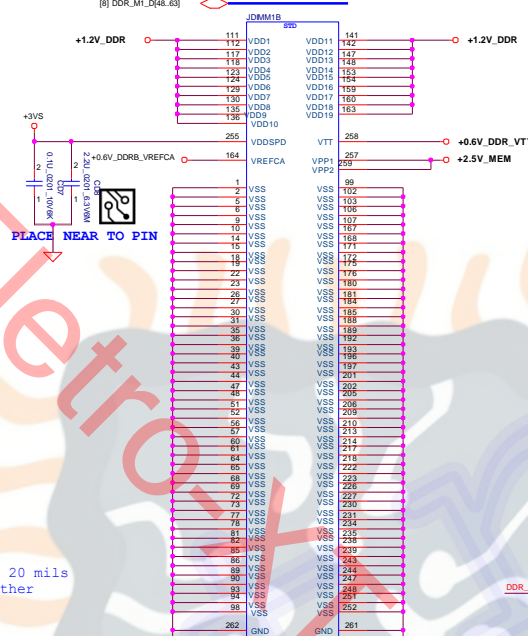
# Non-Interleaved Memory

## CHANNEL-M1

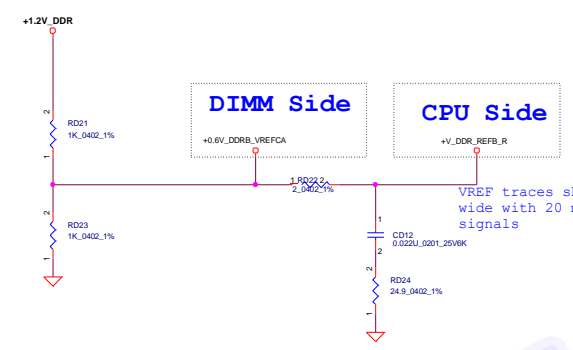
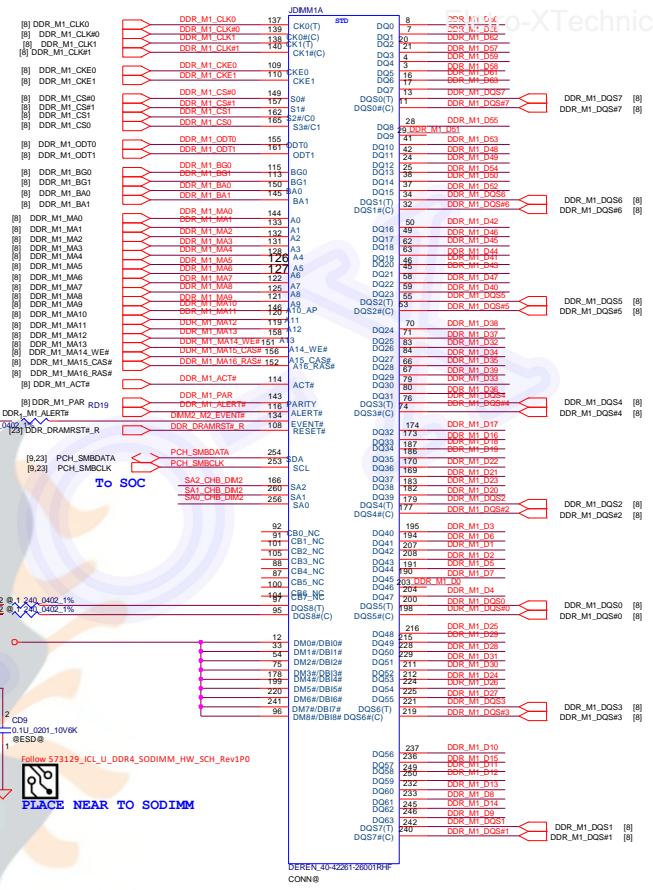
BOT: DIMM2 (JDIMM1 CONN) Non-ECC DIMM



SPD ADDRESS FOR CHANNEL B :  
SA0 = 0; SA1 = 1; SA2 = 0.



PLACE NEAR TO PIN

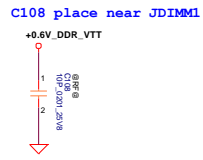
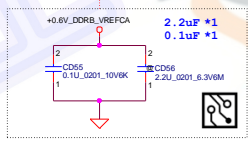
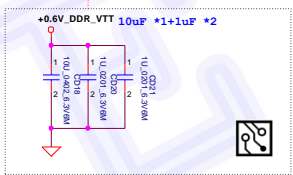
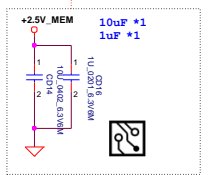


### Decoupling Cap. Channel B

Layout Note:  
Place near JDIMM1.257,259

Layout Note:  
Place near JDIMM1.258

Layout Note:  
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1



Layout Note:  
Place near JDIMM1

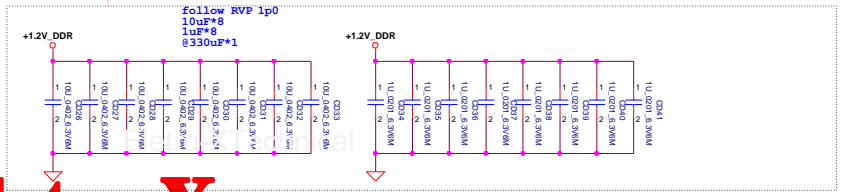
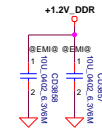


Table 4-26. DDR4 SODIMM Power Plane Decoupling

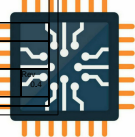
Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)
	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	1x 330 $\mu$ F (7343)
	VTT	Place on VTT plane close to DIMM	2x 10 $\mu$ F (0603)
	VPP	DIMM pin side, 1 per DIMM	2x 10 $\mu$ F (0603)
	VPP	DIMM pin side, 1 per DIMM	2x 1 $\mu$ F (0402)
VDDSPD	VDDSPD	Place close to DIMM	2x 0.1 $\mu$ F (0402)
	VDDSPD	Place close to DIMM	2x 2.2 $\mu$ F (0402)

Note:  
1. Total quantity is referring to 2 channels.

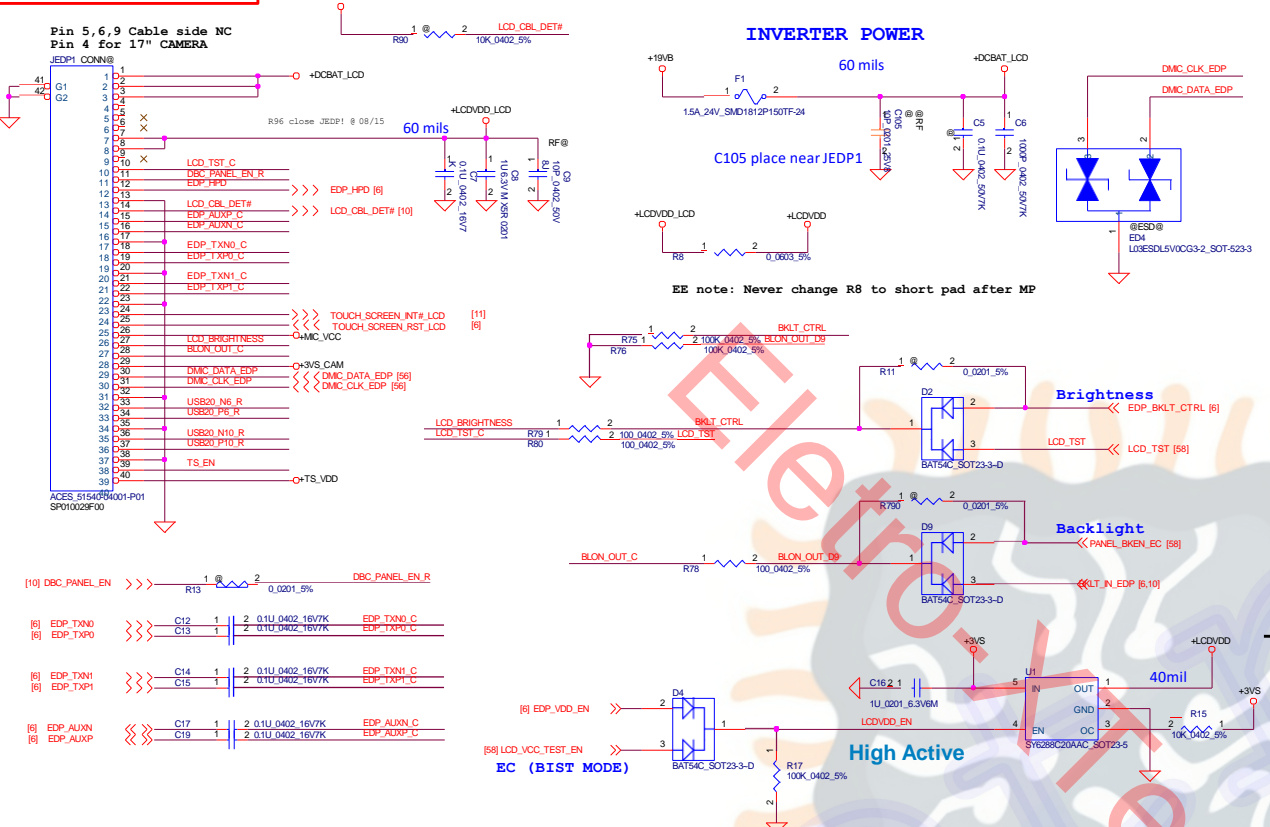


Part Number:SP07001HW0L  
Part Description:S SOCKET LOTES ADDR0205-P001A02 DDR4 A31

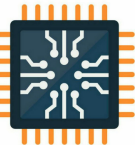
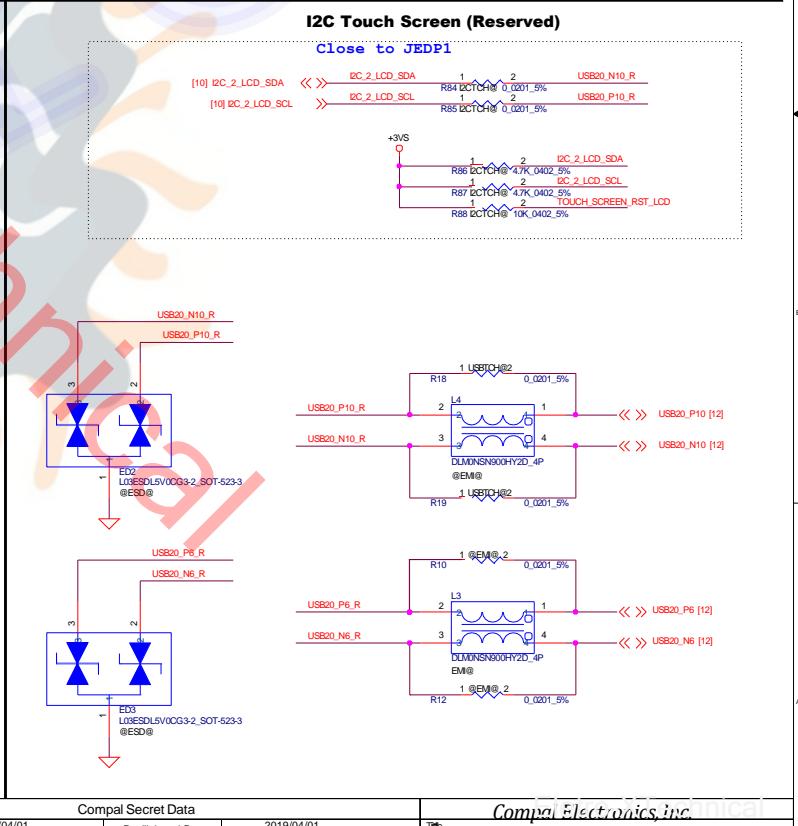
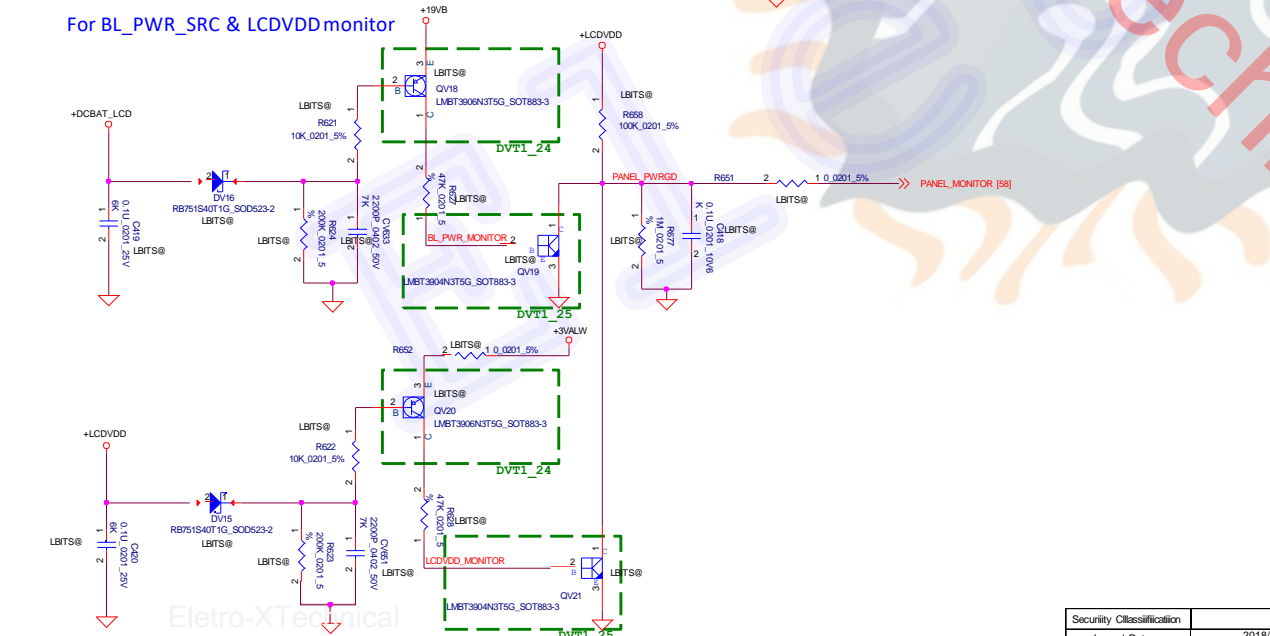
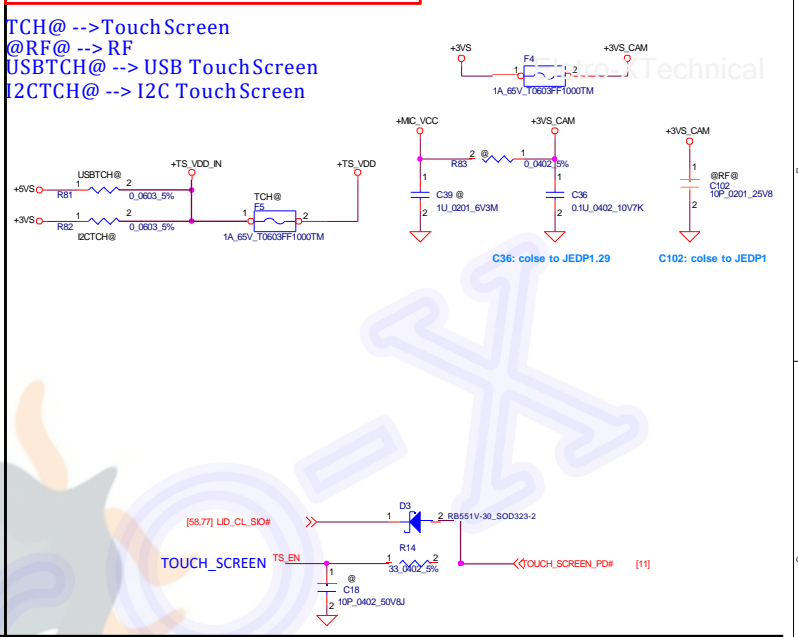
08/30  
Update Table 4-26 for DDR4 80-DIMM Decoupling Caps  
572907\_ICL\_UY\_PDG\_Rev07 Page.99



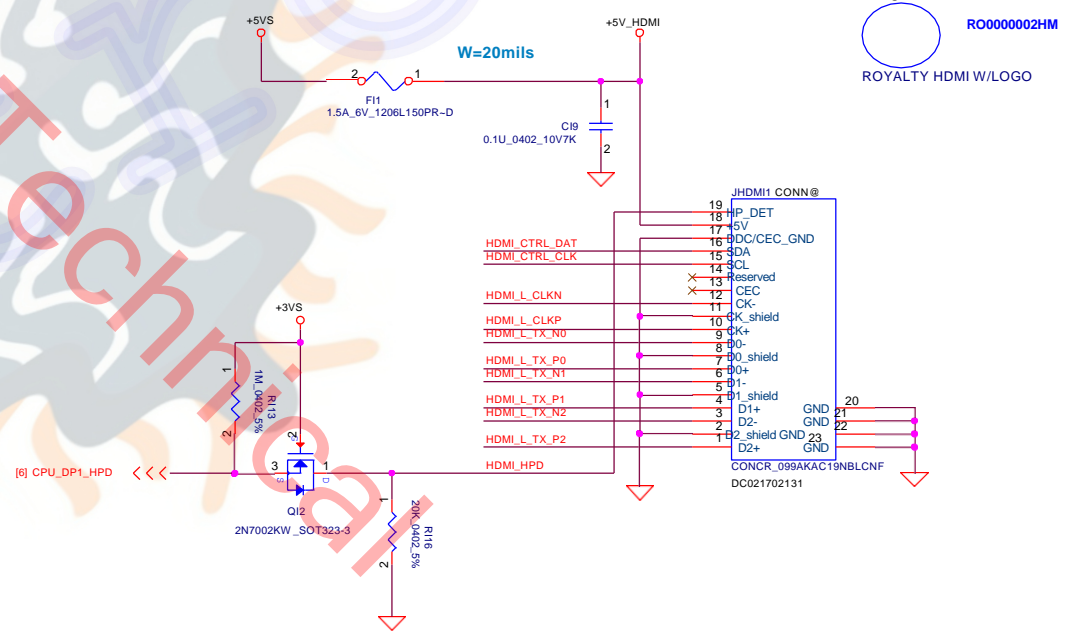
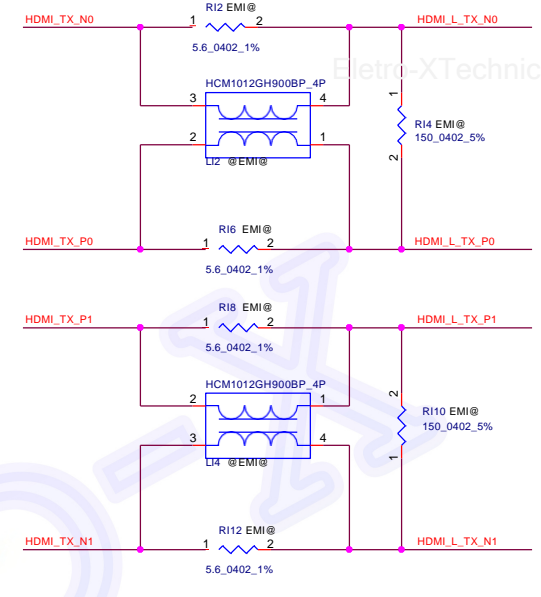
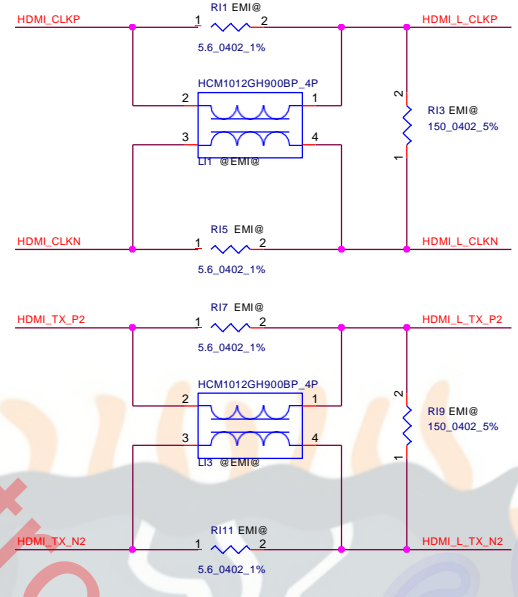
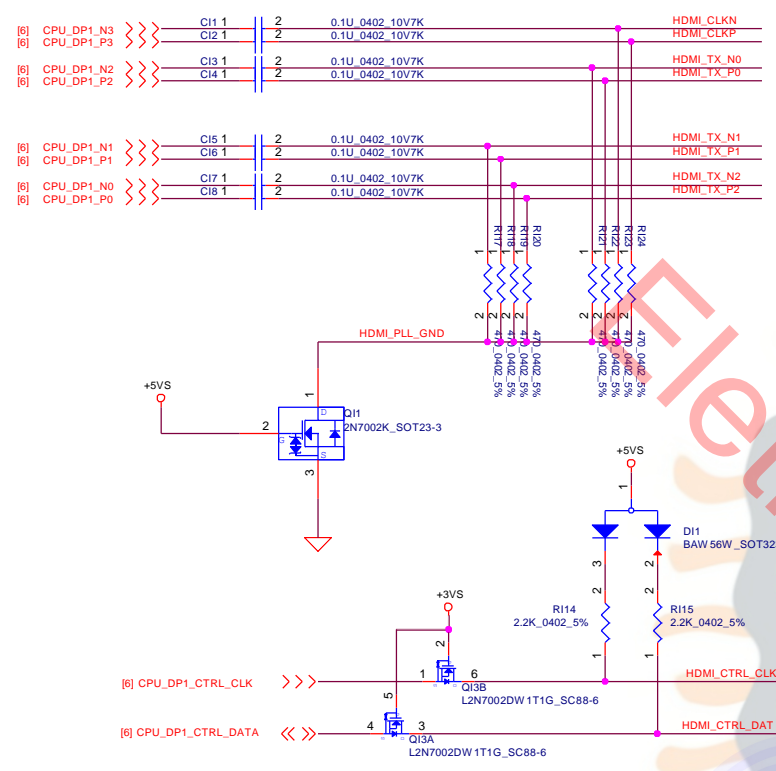
**Main Func = LCD**



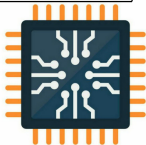
**Main Func = CAM&MIC, TS**



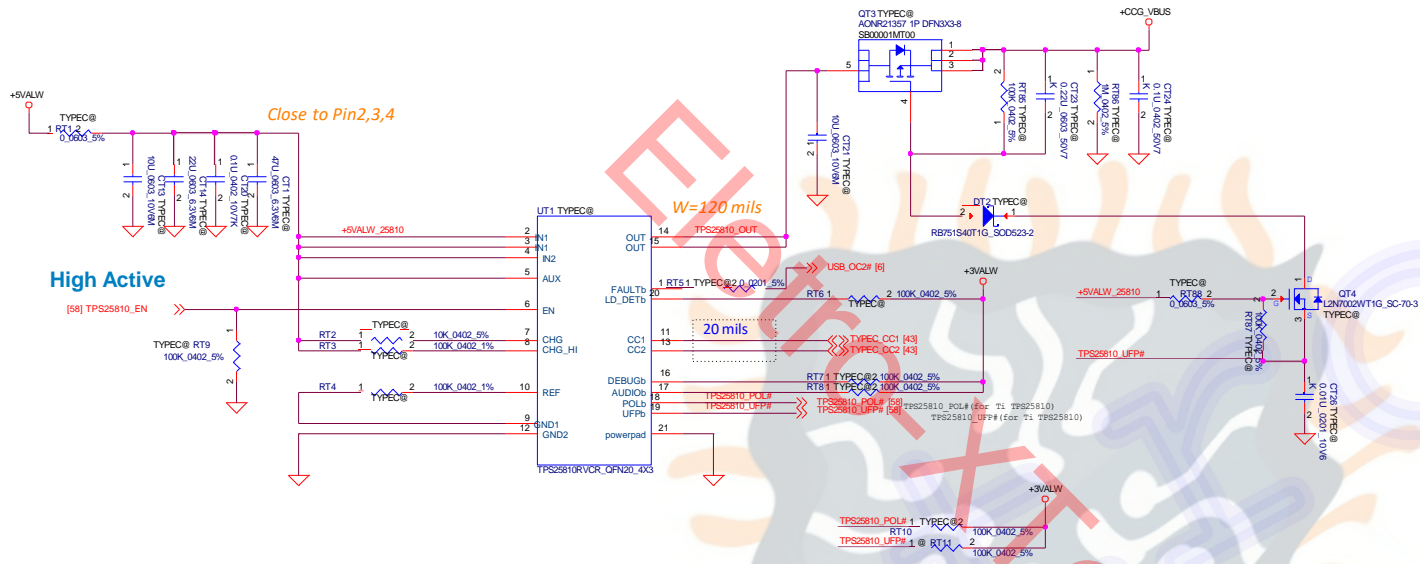
**Main Func = HDMI**



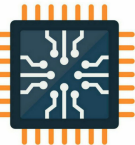
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Issued Date		2018/04/01		Deciphered Date		2019/04/01	
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Title <b>HDMI L Shifter/Conn</b>						Date Monday, JUN 29, 2019	
Size Document Number <b>LA-J091P</b>						Sheet 40 of 101	



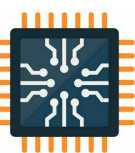
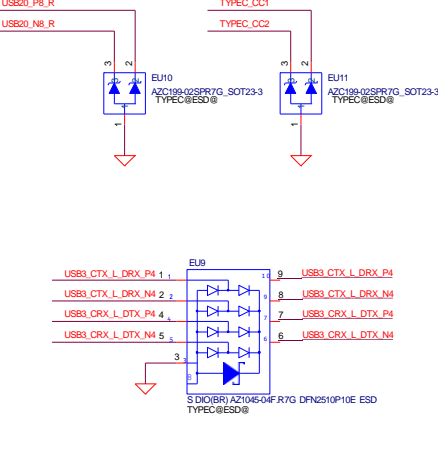
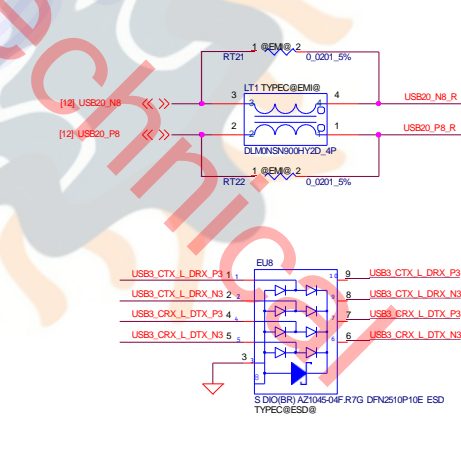
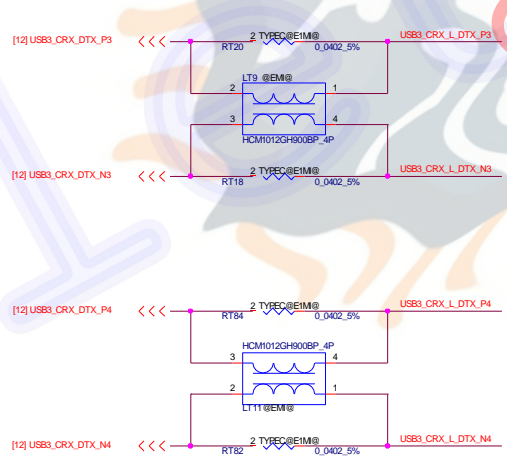
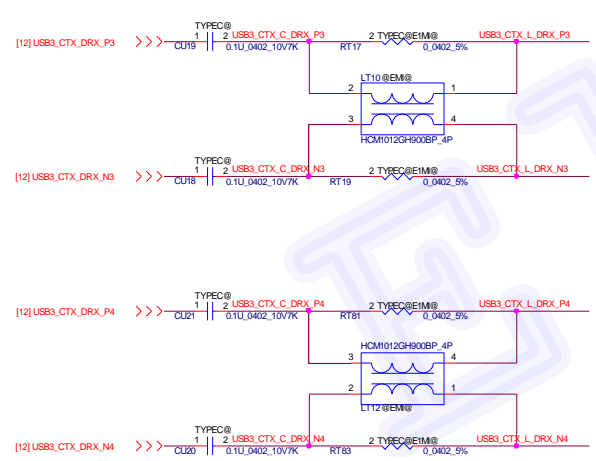
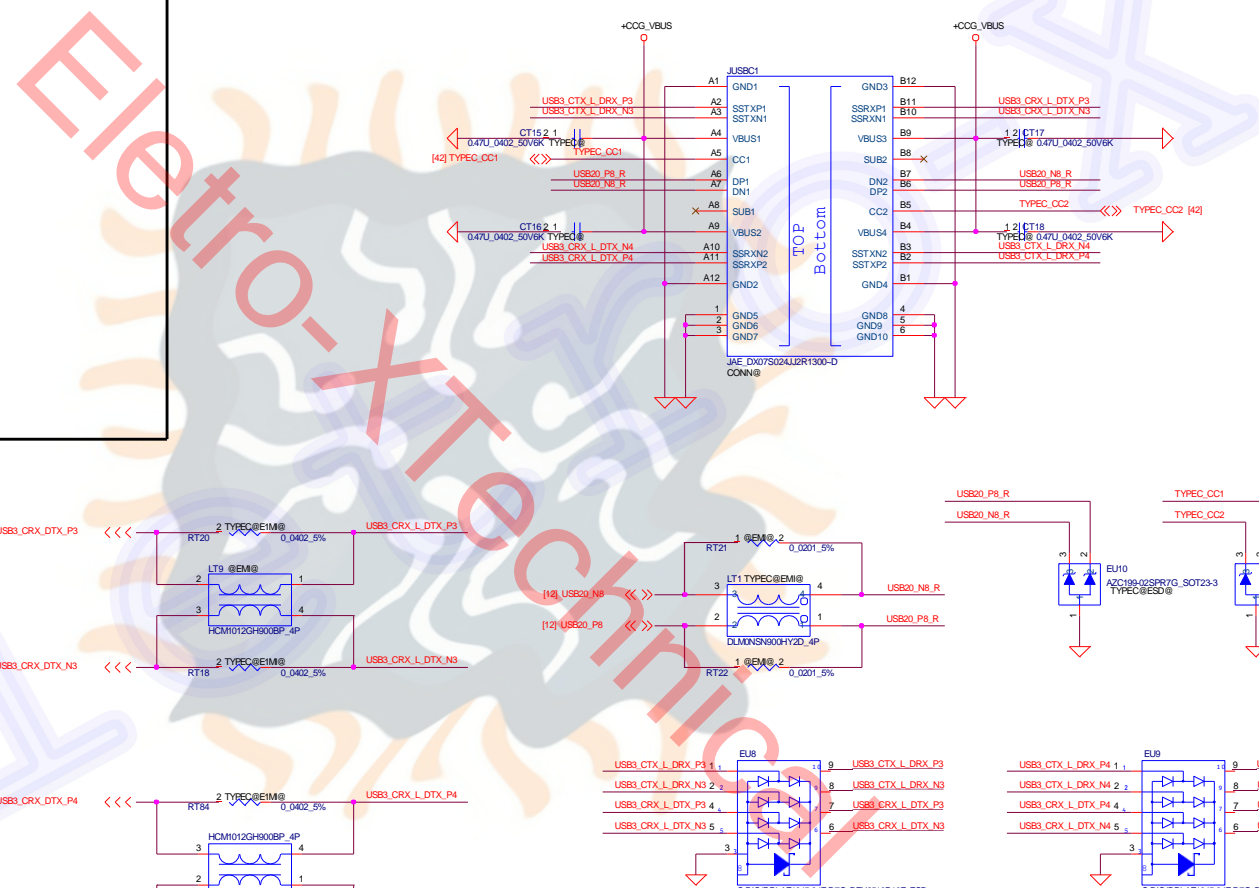
5V@3A

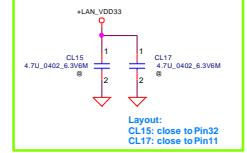
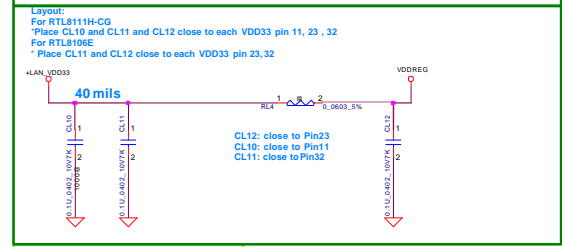
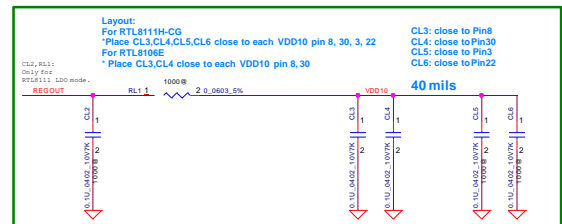


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Sketch/Document Number				Rev
LA-J091P				0.2
Date	Monday, July 23, 2019	Sheet	42 of 101	

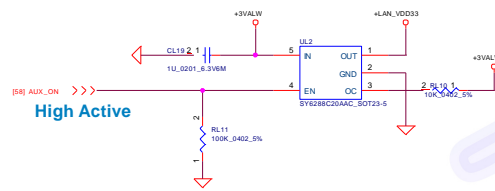
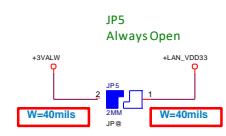






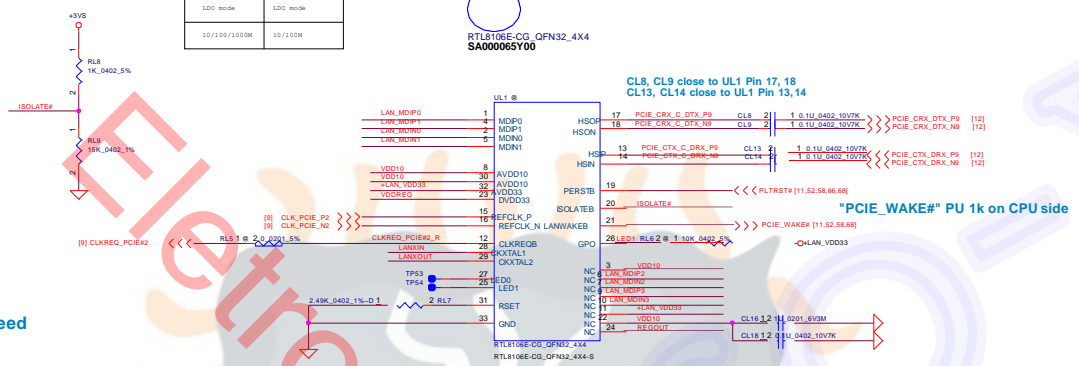
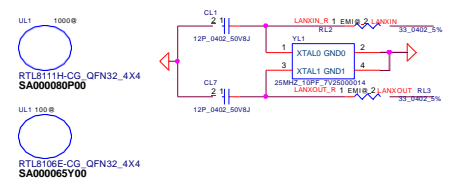


**+LAN\_VDD33 Rising time (10%-90%) need >0.5mS and <100mS.**

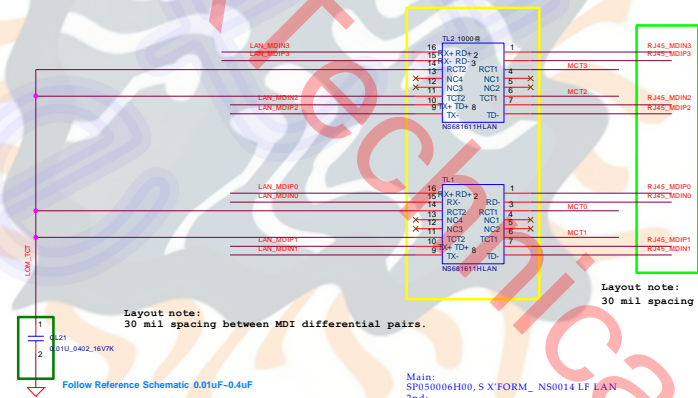


**LAN CHIP 10/100/1000**

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000063Y00
LDO mode	LDO mode
10/100/1000M	10/100M



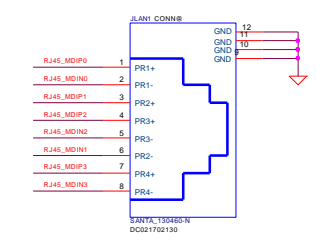
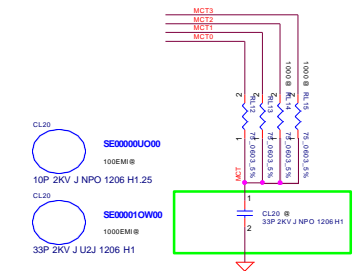
**Main Func = LAN LAN TransFormer 10/100M x2**



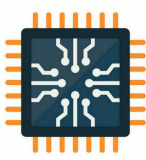
**TL1 TOP, TL1 BOT**

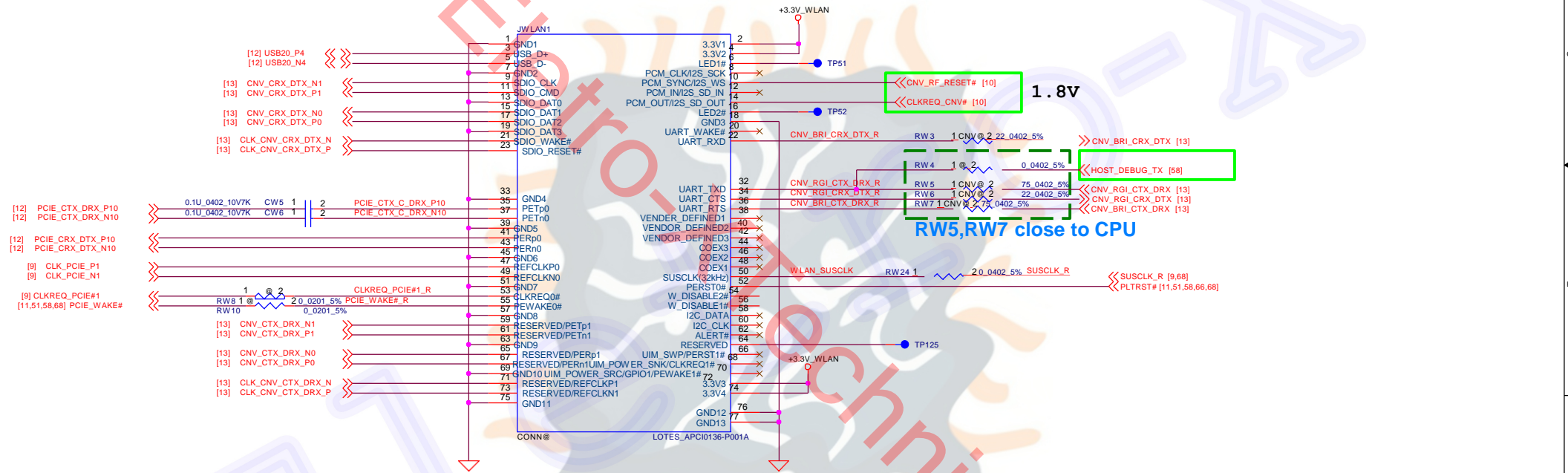
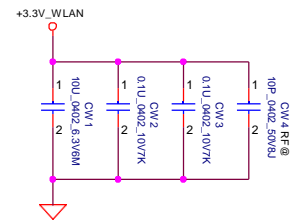
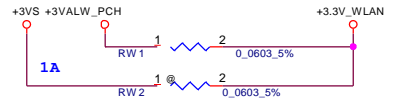
**Layout note:**  
30 mil spacing between MDI differential pairs.

	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

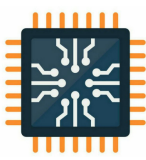


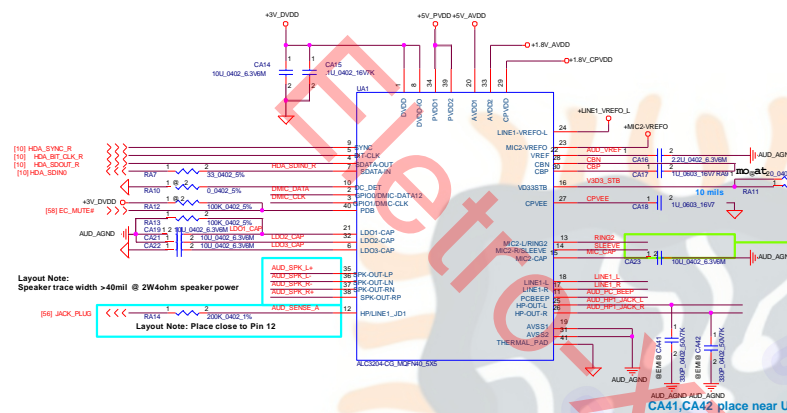
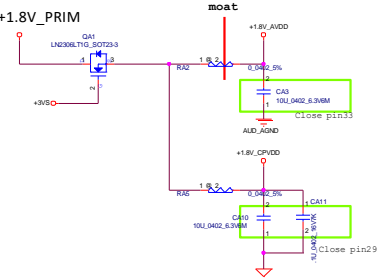
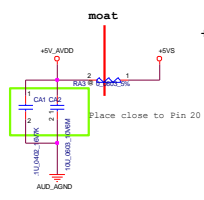
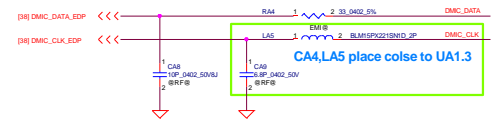
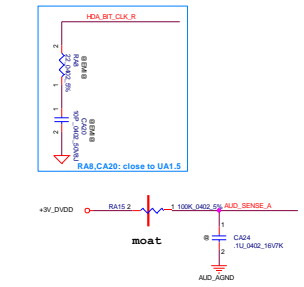
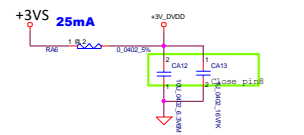
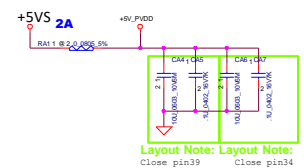
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Size Document Number				Rev
LA-J091P				0.2
Date:	Monday, Jm29, 2019	Sheet	52 of 101	





Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

Layout Note: Place close to Pin 12

Layout Note: Width>40mil, to improve Headphone Crosstalk noise Change to 40mil will be better. Add 2 via @0.5A when trace layer change.

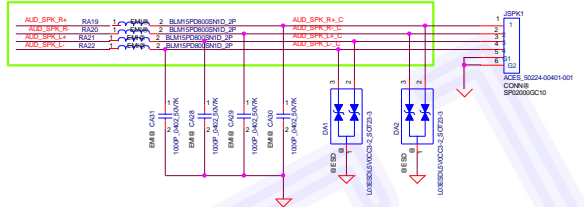
CA41,CA42 place near UA1

Place on the moat between GND & GNDA.

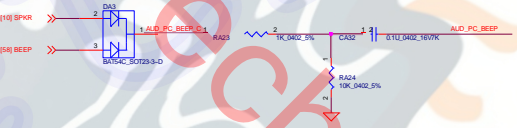


Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

**Speaker**



CONN	Pin	Net name
P1.n1	1	SPK_+
P1.n2	2	SPK_-
P1.n3	3	SPK_L+
P1.n4	4	SPK_L-

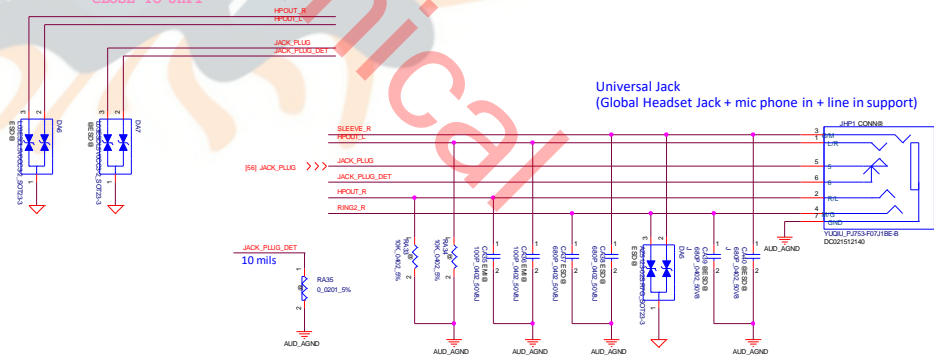


**Main Func = Audio Jack**

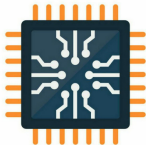
Universal Jack (Global Headset Jack + mic phone in + line in support)



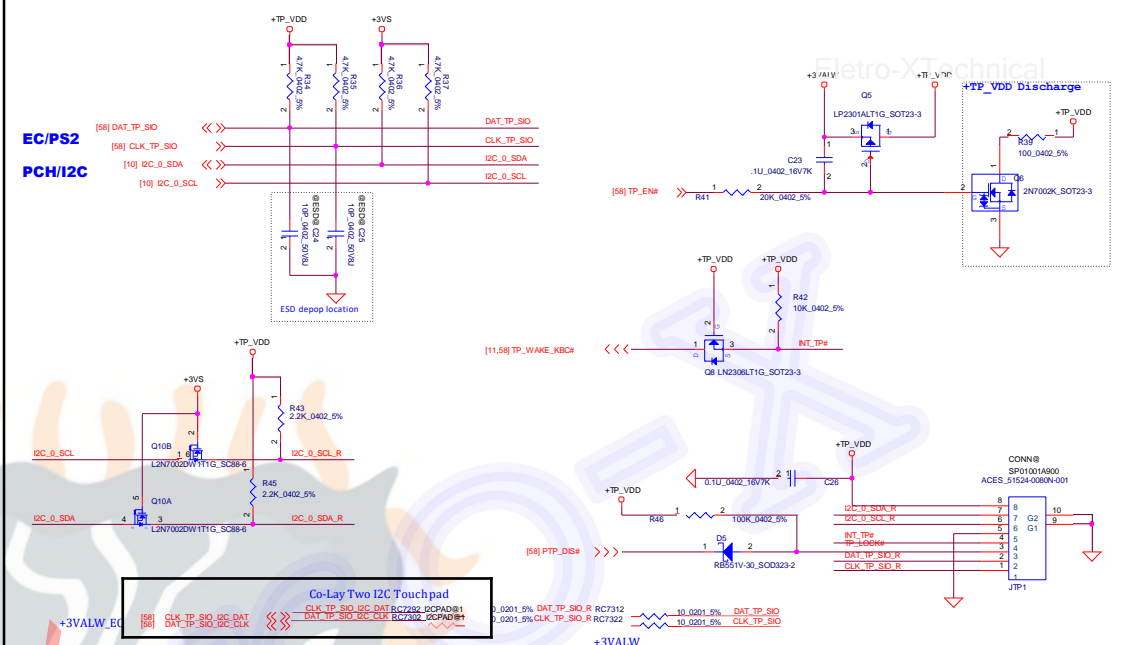
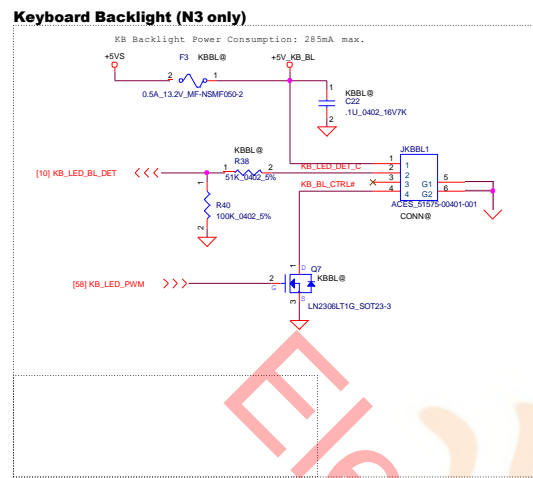
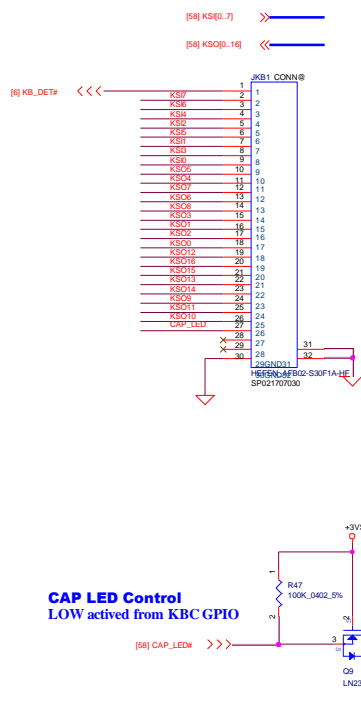
Layout Note: Close to UA1



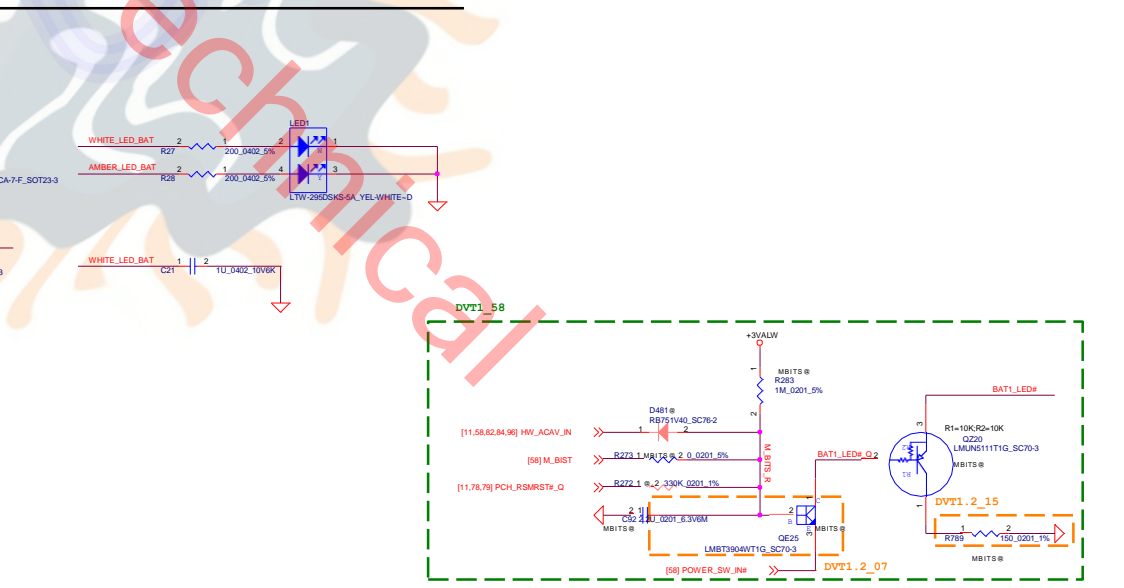
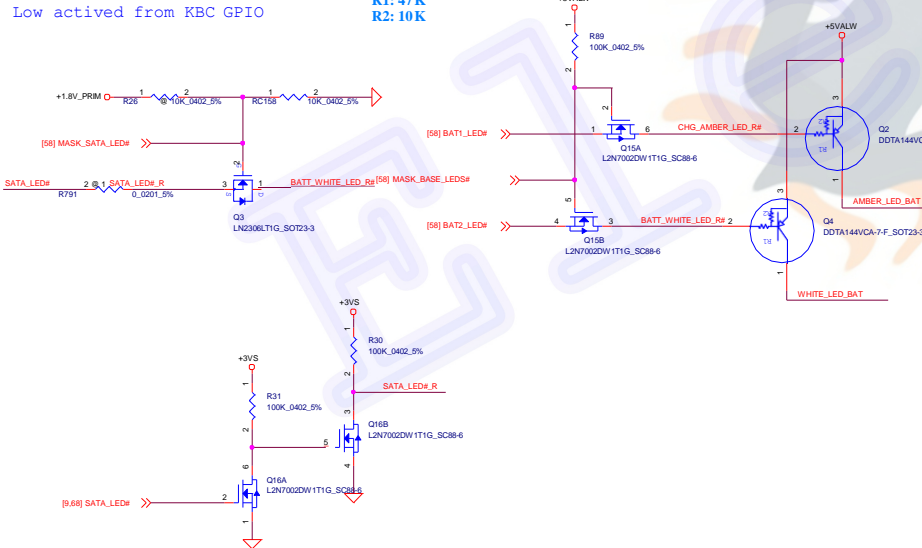
Universal Jack (Global Headset Jack + mic phone in + line in support)



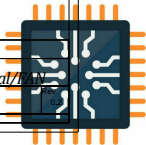




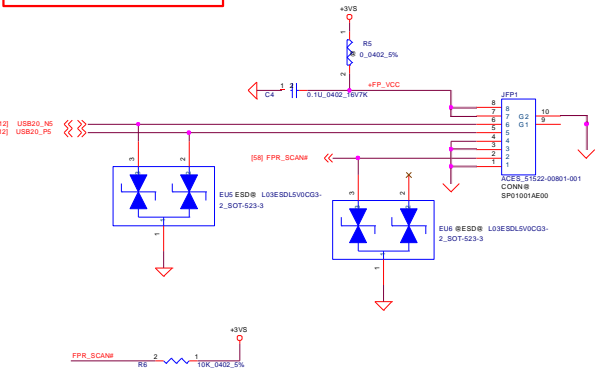
Main Func = Battery LED



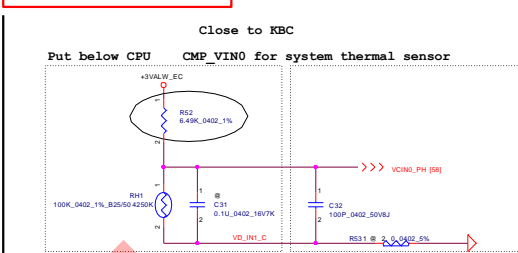
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Issued Date	2018/04/01	Deciphered Date
2019/04/01		2019/04/01



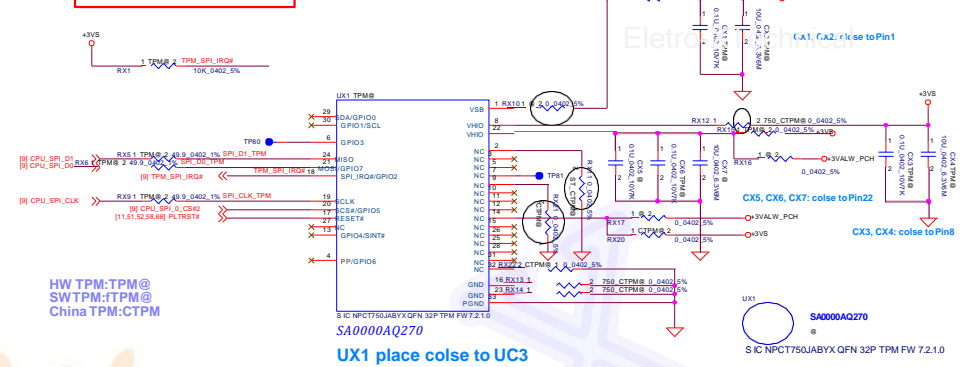
**Main Func = FPR**



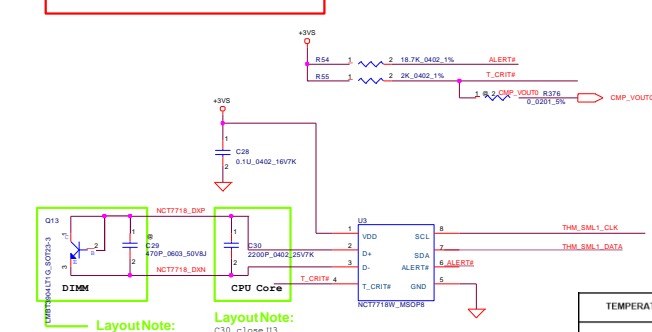
**Main Func = OTP**



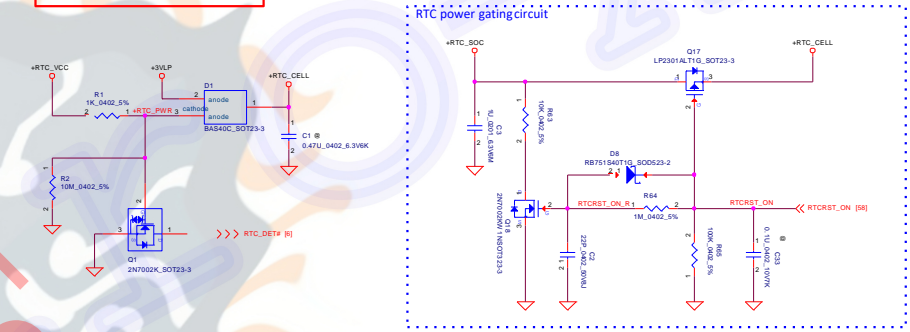
**Main Func = TPM**



**Main Func = Thermal**

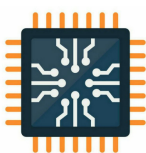


**Main Func = RTC**

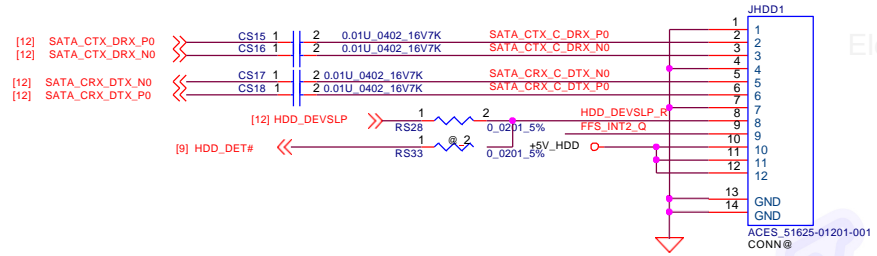
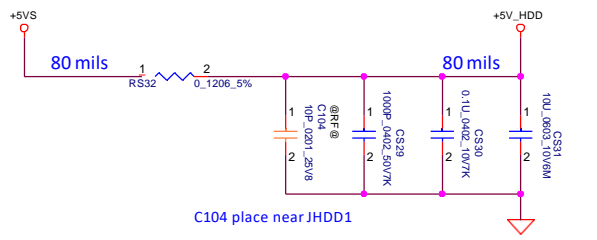


LayoutNote: DXM and DXP routing width and spacing is 10 mil / 10 mil.

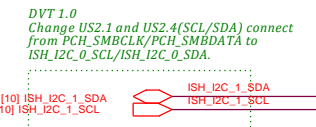
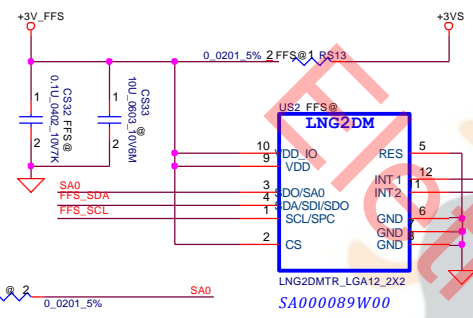
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Issued Date	2019/04/01	Deciphered Date	2019/04/01
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# Main Func = HDD&FFS

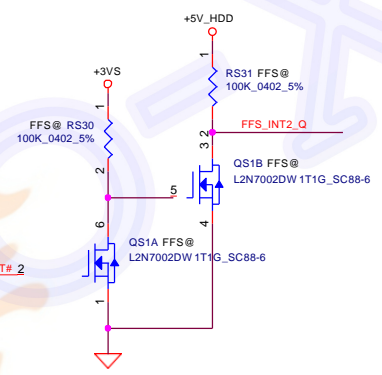


CONN	FFC
GND	S1 1
A+	S2 2
A-	S3 3
GND	S4 4
B-	S5 5
B+	S6 6
GND	S7 7
DEVS_LP	P3 8
5V	P7 10
5V	P8 11
5V	P9 12
GND	P10
Device Activity	P11 9

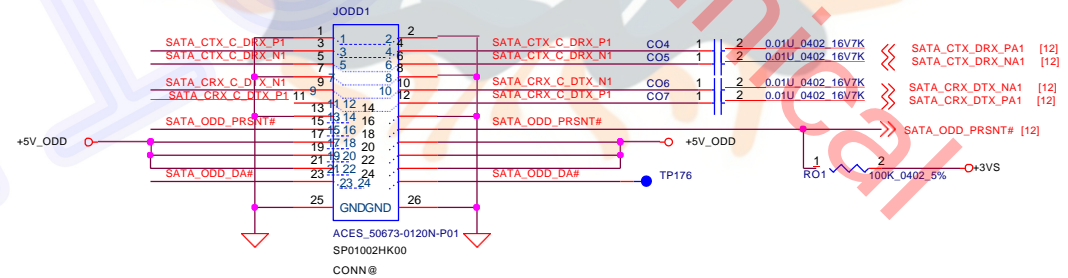
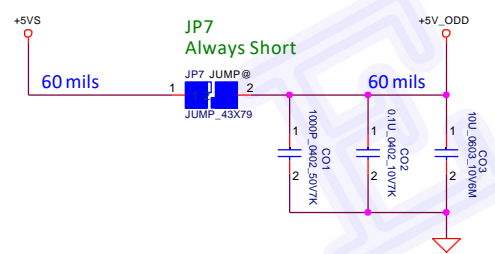


DVT 1.0  
Change US2.1 and US2.4(SCL/SDA) connect from PCH\_SMBCLK/PCH\_SMBDATA to ISH\_I2C\_0\_SCL/ISH\_I2C\_0\_SDA.

DVT 1.0  
Change US2.3 (SA0) connect from +3V\_FFS to GND.



# Main Func = ODD



CONN	FFC
GND	S1 1
A+	S2 2
A-	S3 3
GND	S4 4
B-	S5 5
B+	S6 6
GND	S7 7
PRSENT	P1 8
5V	P2 9
5V	P3 10
Attention	P4 12
GND	P5
GND	P6

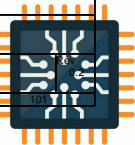
Security Classification	Compal Secret Data	
Issued Date	2018/04/01	Deciphered Date
		2019/04/01

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Title		Compal Electronics, Inc.	
Size		Document Number	
Custom		LA-G711P	
Date:	Monday, July 29, 2019	Sheet	67 of 101

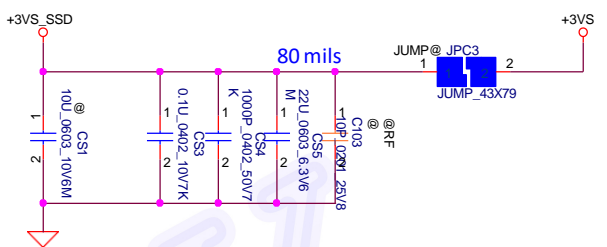


Eleto-X Technical

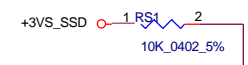
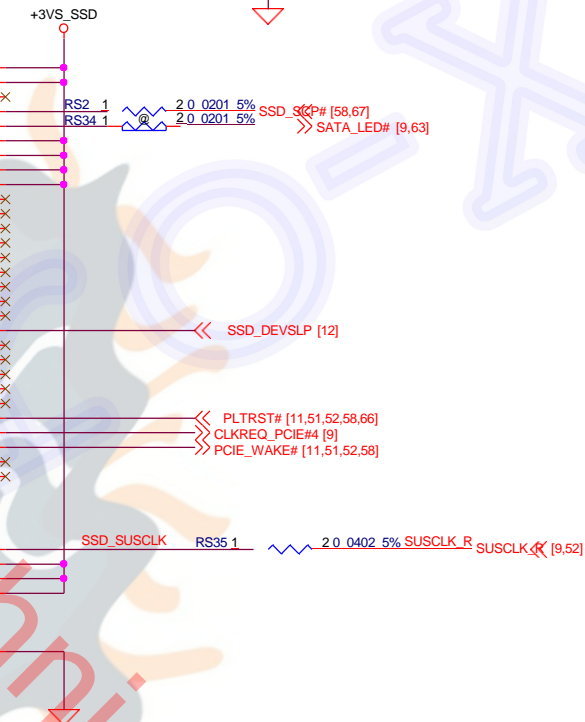
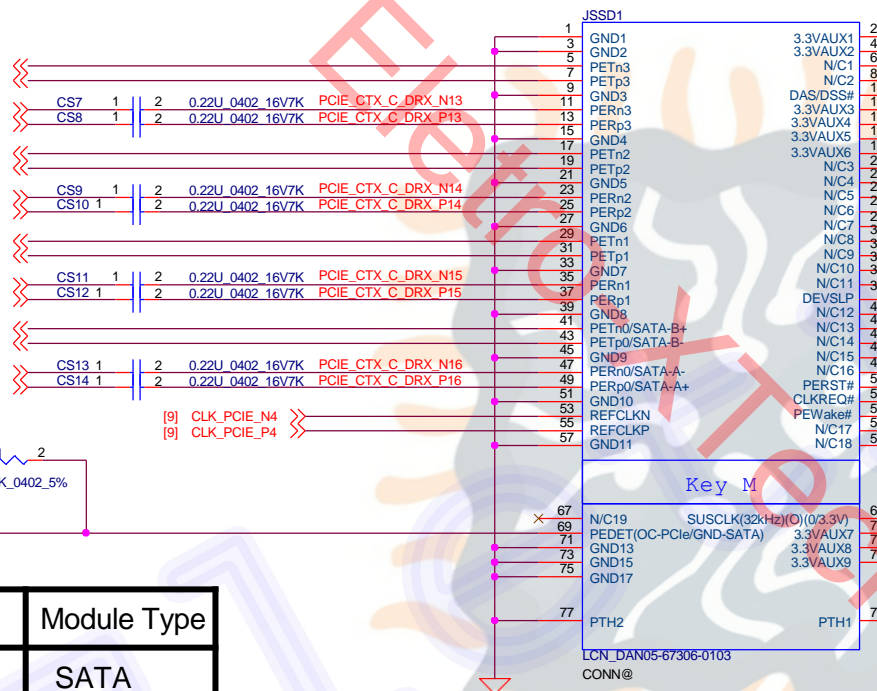




NGFF Key M

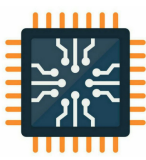


- [12] PCIE\_CRX\_DTX\_N13
- [12] PCIE\_CRX\_DTX\_P13
- [12] PCIE\_CRX\_DTX\_N14
- [12] PCIE\_CRX\_DTX\_P14
- [12] PCIE\_CRX\_DTX\_N15
- [12] PCIE\_CRX\_DTX\_P15
- [12] PCIE\_CRX\_DTX\_N16
- [12] PCIE\_CRX\_DTX\_P16



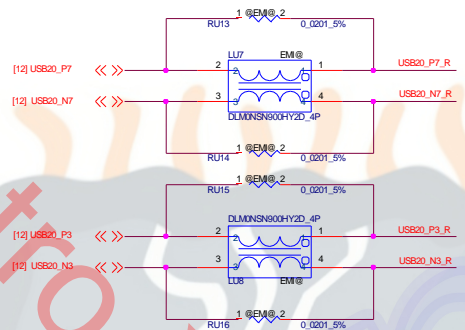
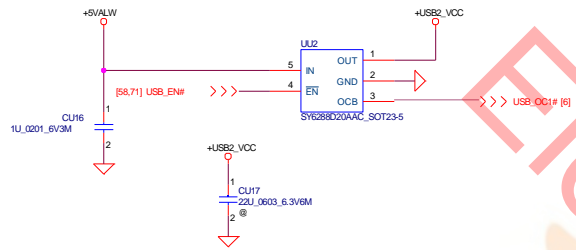
PEDET	Module Type
0	SATA
1	PCIE

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				Document Number
				Rev
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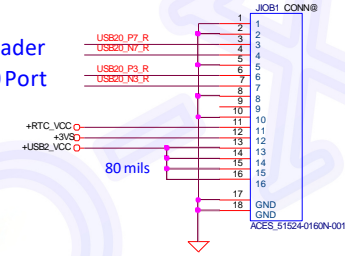


Main Func = USB2.0 Port3 + Card Reader on IO/B

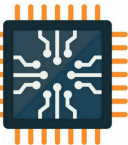


USB2.0/Card Reader connector

CardReader  
USB2.0 Port

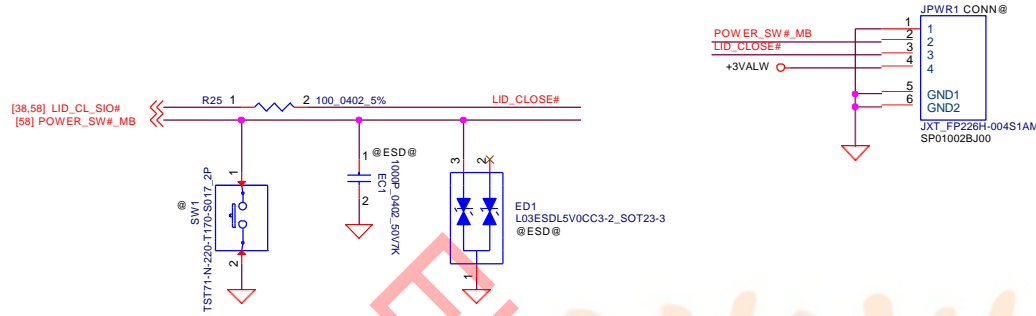


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Date: Monday, July 23, 2018				Sheet	73 of 101

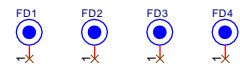
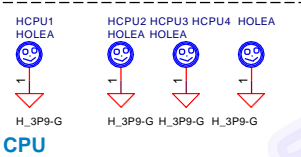
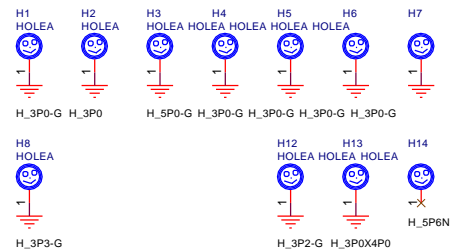


**Main Func = Power BTN**

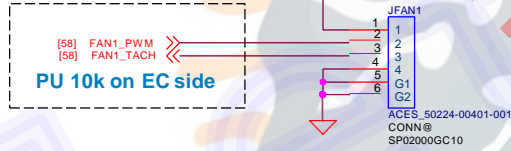
Low actived from KBC GPIO



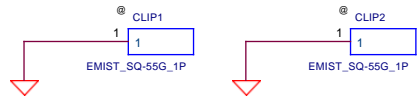
**Screw hole/FD**



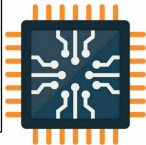
**FAN**



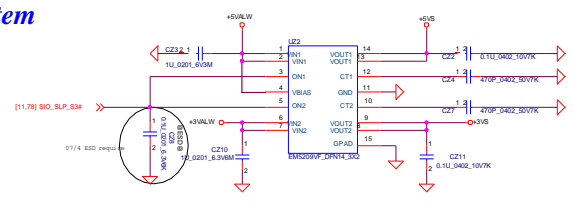
**PCB PN**



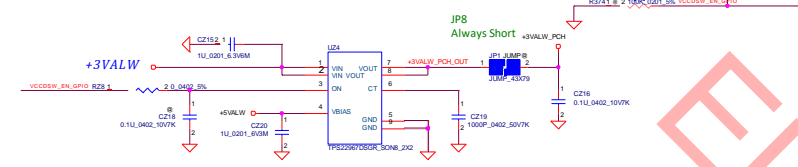
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Rev			0.2	
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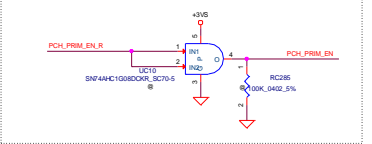
**+5VS / +3VS for System**



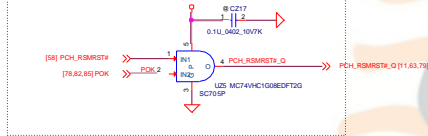
**+3VALW TO +3VALW\_PCH**



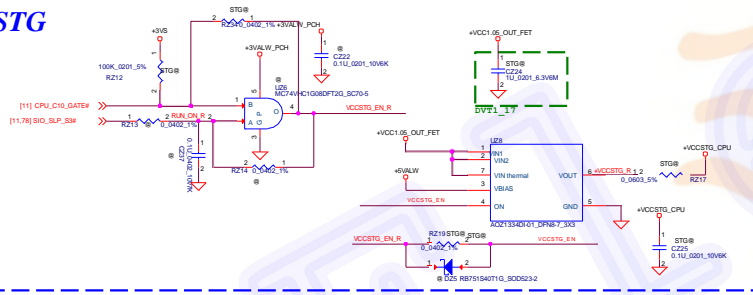
**PCH\_PRIM\_EN**



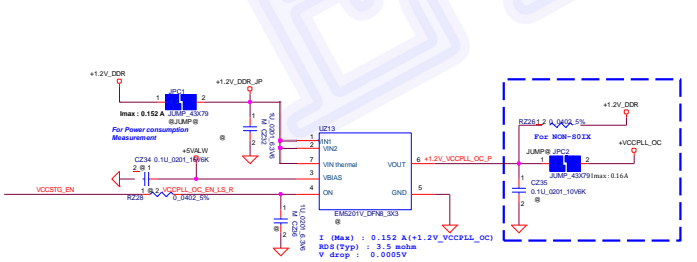
**RSMRST circuit**



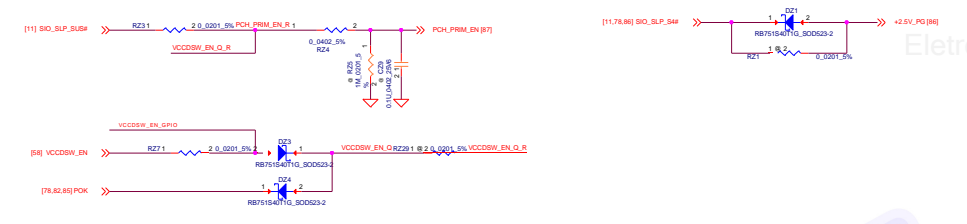
**VCCSTG**



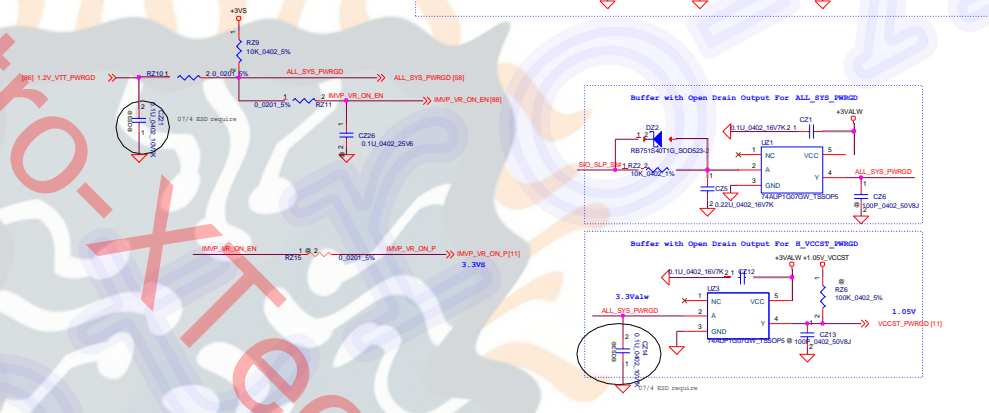
**+1.2V\_VDDQ TO +1.2V\_VCCPLL\_OC**



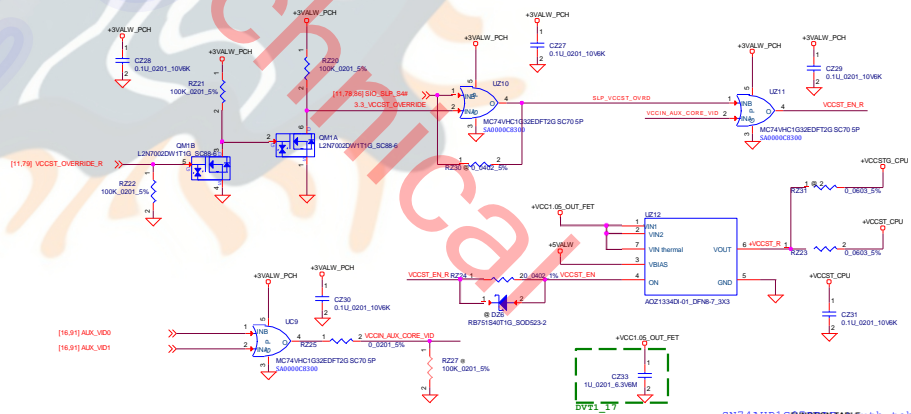
**Sequence Logic**



**IMVP\_VR\_ON&VCCST\_PWRGD**

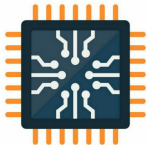


**VCCST**

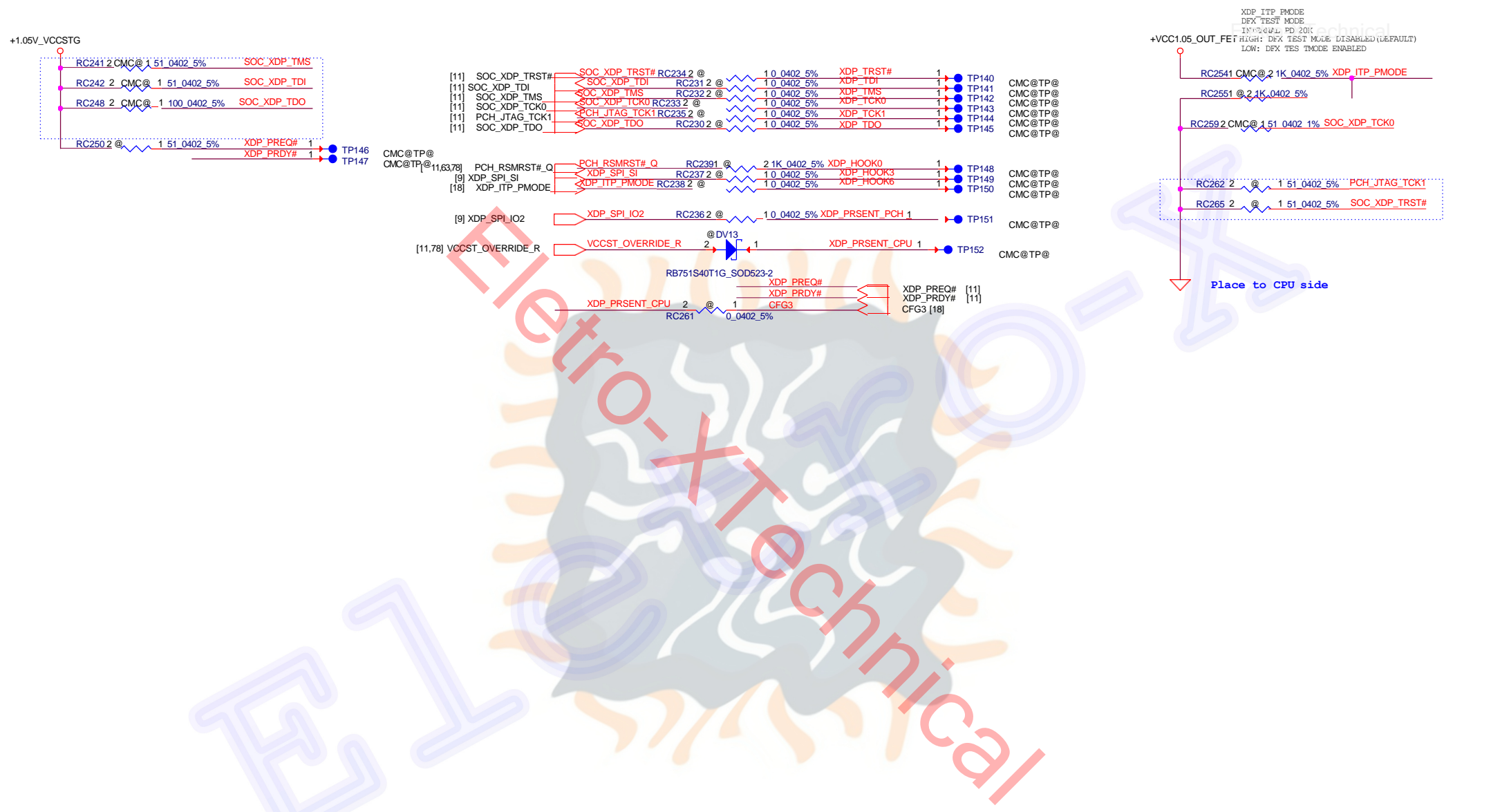


SN74AUP1 FUNCTION TABLE with table

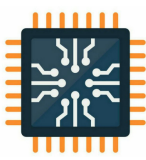
INPUTS	A	OUTPUT
L	L	L
L	L	L
L	H	H
L	H	H
H	L	L
H	L	L
H	H	H
H	H	H



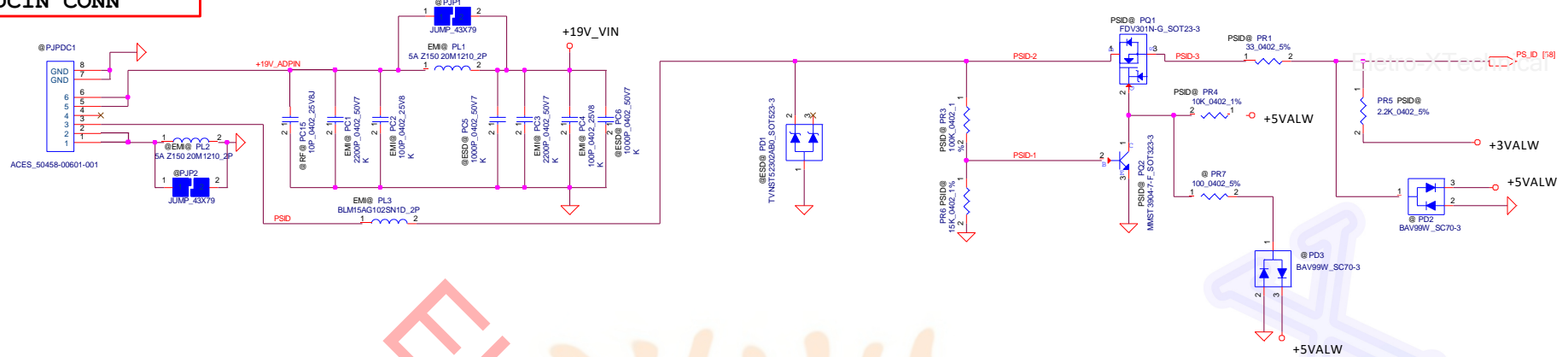
# Main Func = Power Monitor



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				Date: Tuesday, July 30, 2019	Sheet 79 of 101



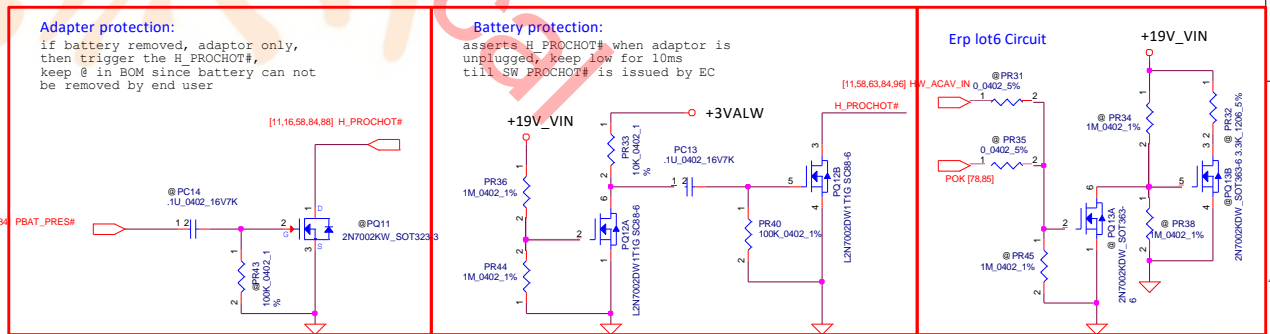
**Main Func = DCIN CONN**



**Battery Bot Side**

- PIN1 GND
- PIN2 GND
- PIN3 GND
- PIN4SYS\_PRES
- PIN5\_BATT\_PRES
- PIN6\_DAT\_SMB
- PIN7\_CLK\_SMB
- PIN8 Batt+
- PIN9 Batt+
- PIN10 Batt+
- SPO21412220

ACES\_50458-01001-P01\_10P-T



Eleto-XTechnical

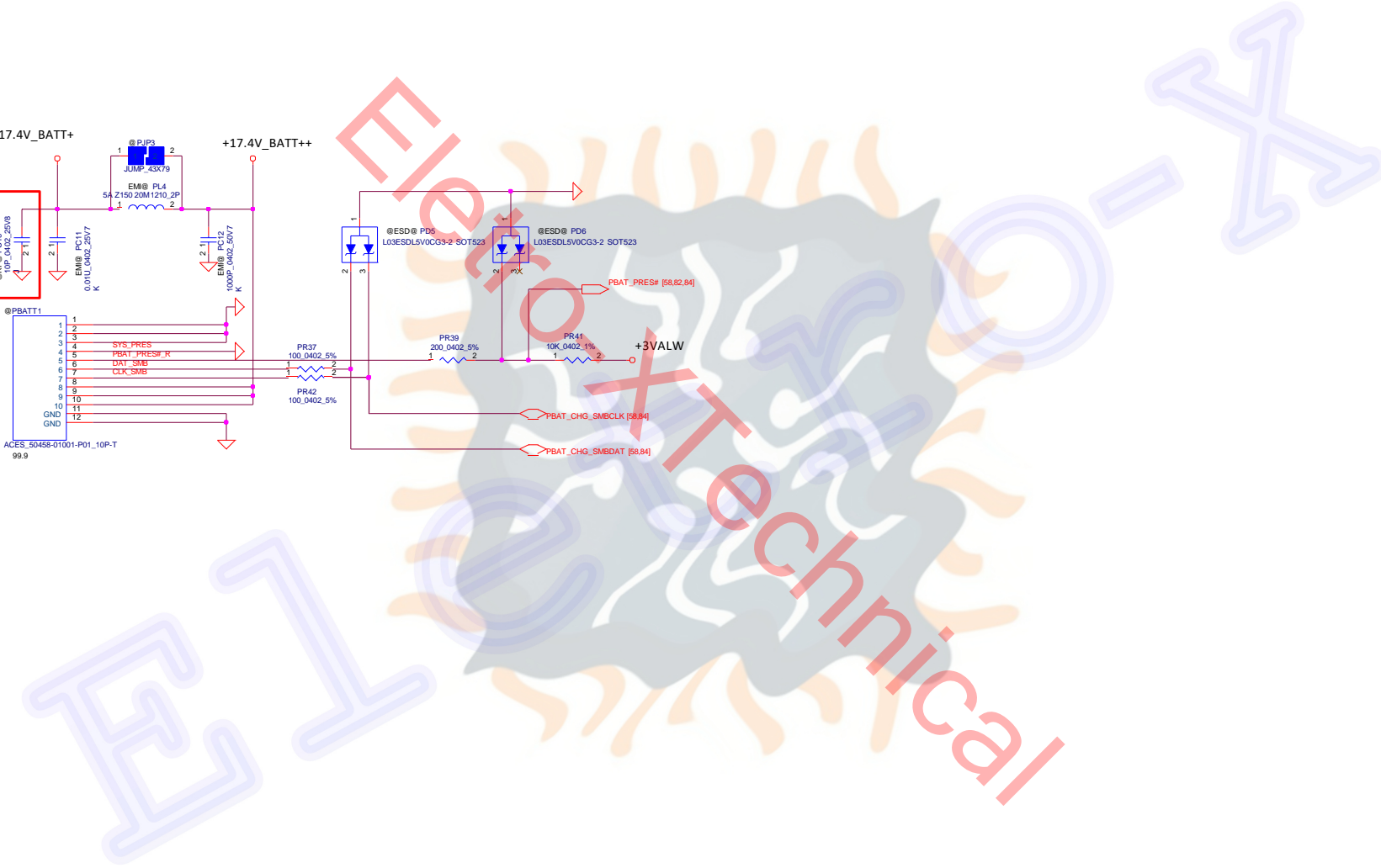
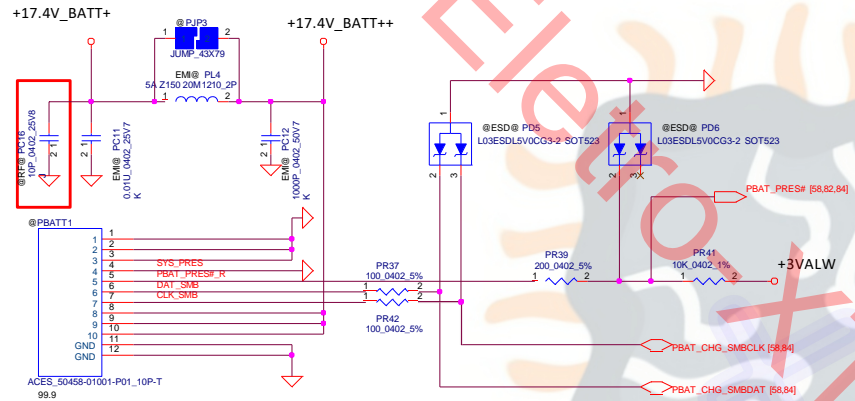
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Title				PWR_DCIN_CONN	
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				Sheet 82 of 100	



Battery Bot Side

- PIN1 GND
- PIN2 GND
- PIN3 GND
- PIN4SYS\_PRES
- PIN5 BATT\_PRS
- PIN6 DAT\_SMB
- PIN7 CLK\_SMB
- PIN8 Batt+
- PIN9 Batt+
- PIN10 Batt+
- SPO21412220

ACES\_50458-01001-P01\_10P-T

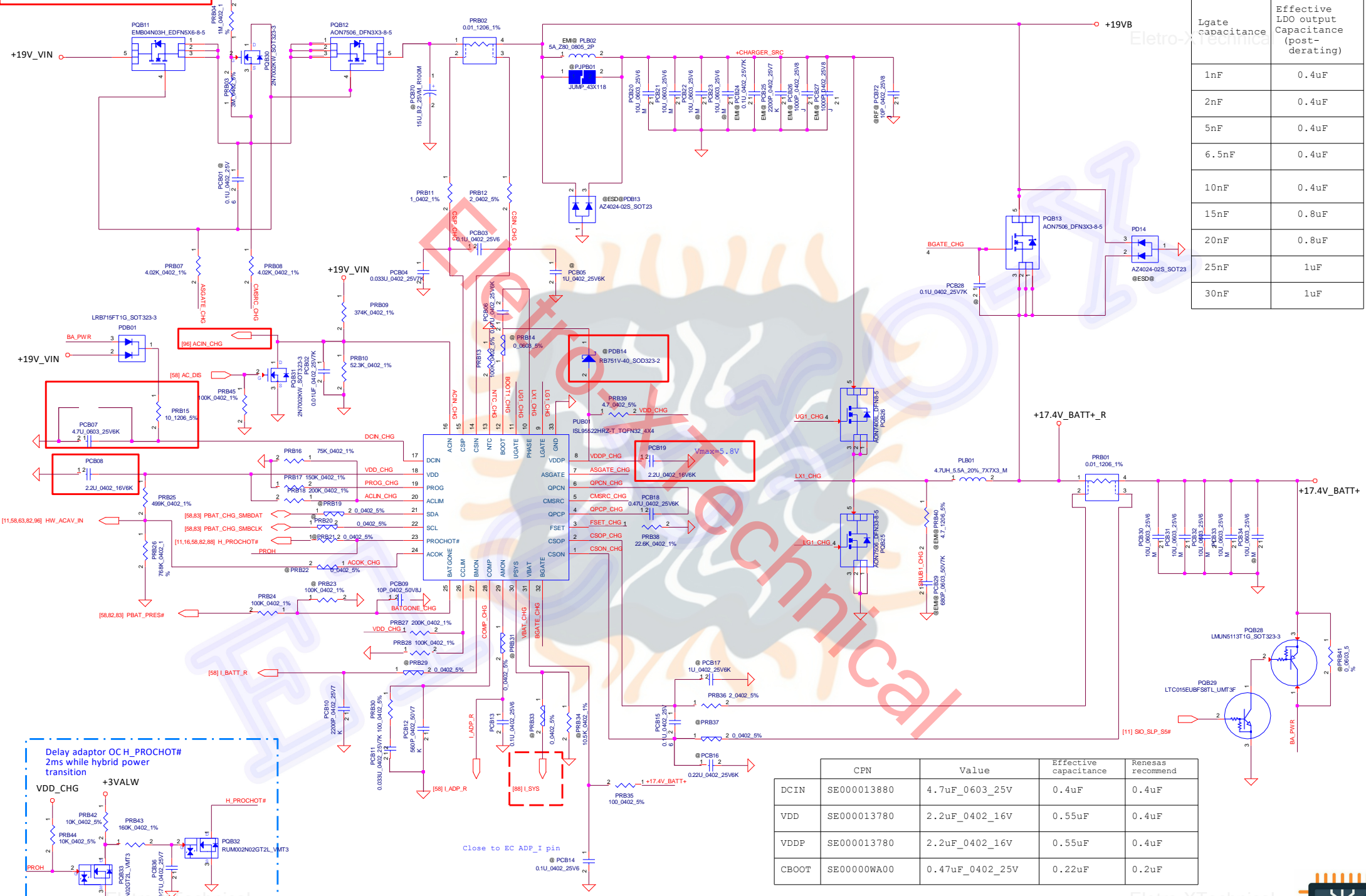


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				Document Number
				Date: Monday, July 23, 2019 [Sheet 83 of 100]



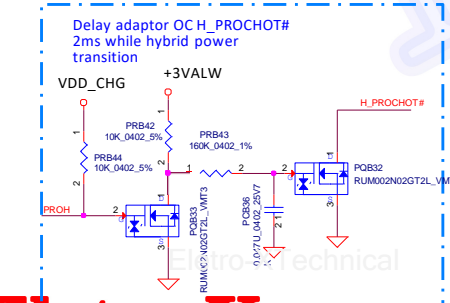


**Main Func = CHARGER**



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.2uF



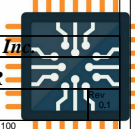
LA-F611PR01\_0531B.DSN  
I\_SYS change to TSENSE\_PSYS (P.72 PUZ01.24)

Security Classification: **Compal Secret Data**

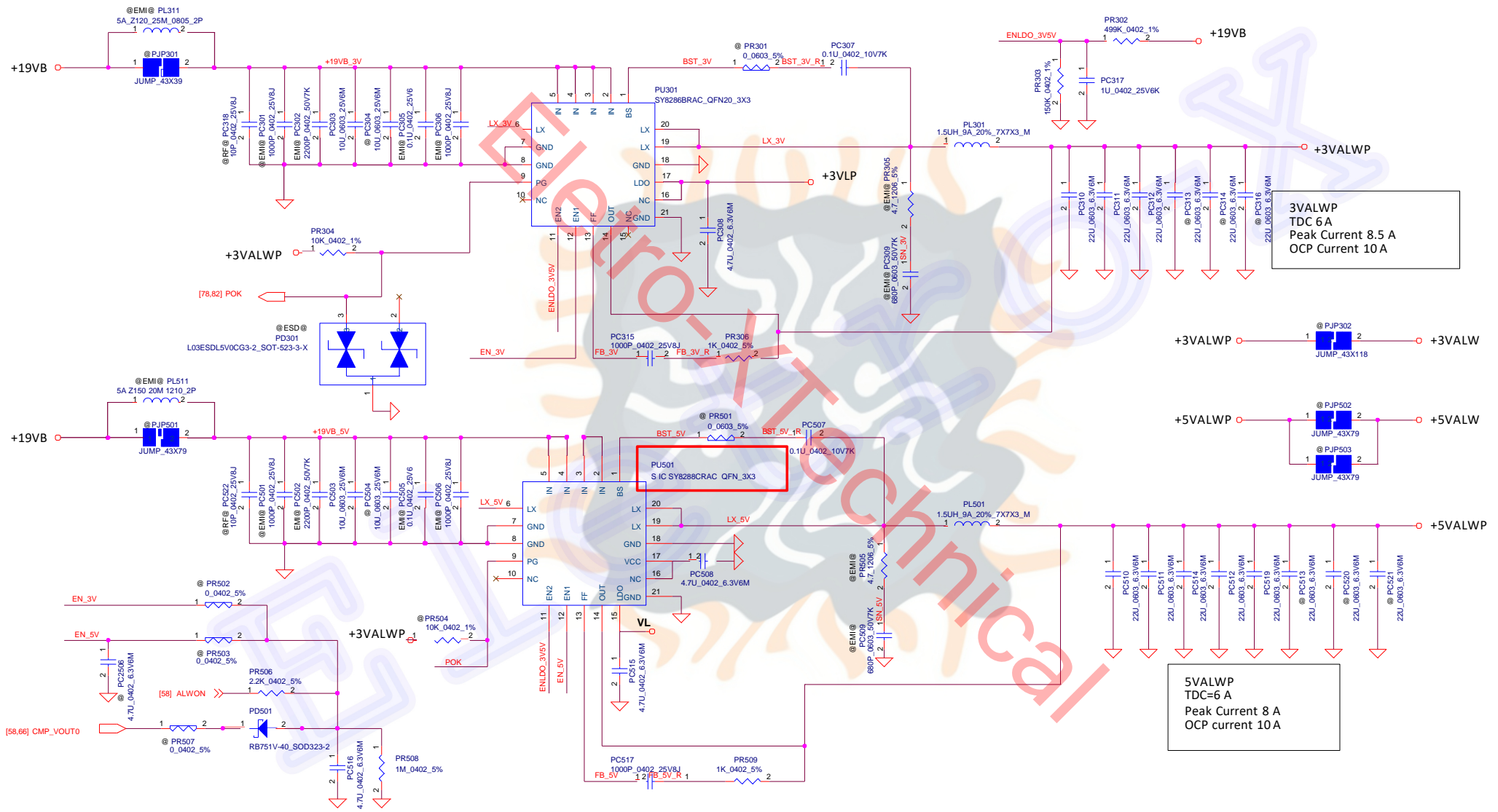
Issued Date: 2016/01/06 | Deciphered Date: 2017/01/06

Document Number: **LA-G712P**

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**Main Func = 3.3VALWP/5VALWP**

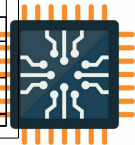


3VALWP  
TDC 6 A  
Peak Current 8.5 A  
OCP Current 10 A

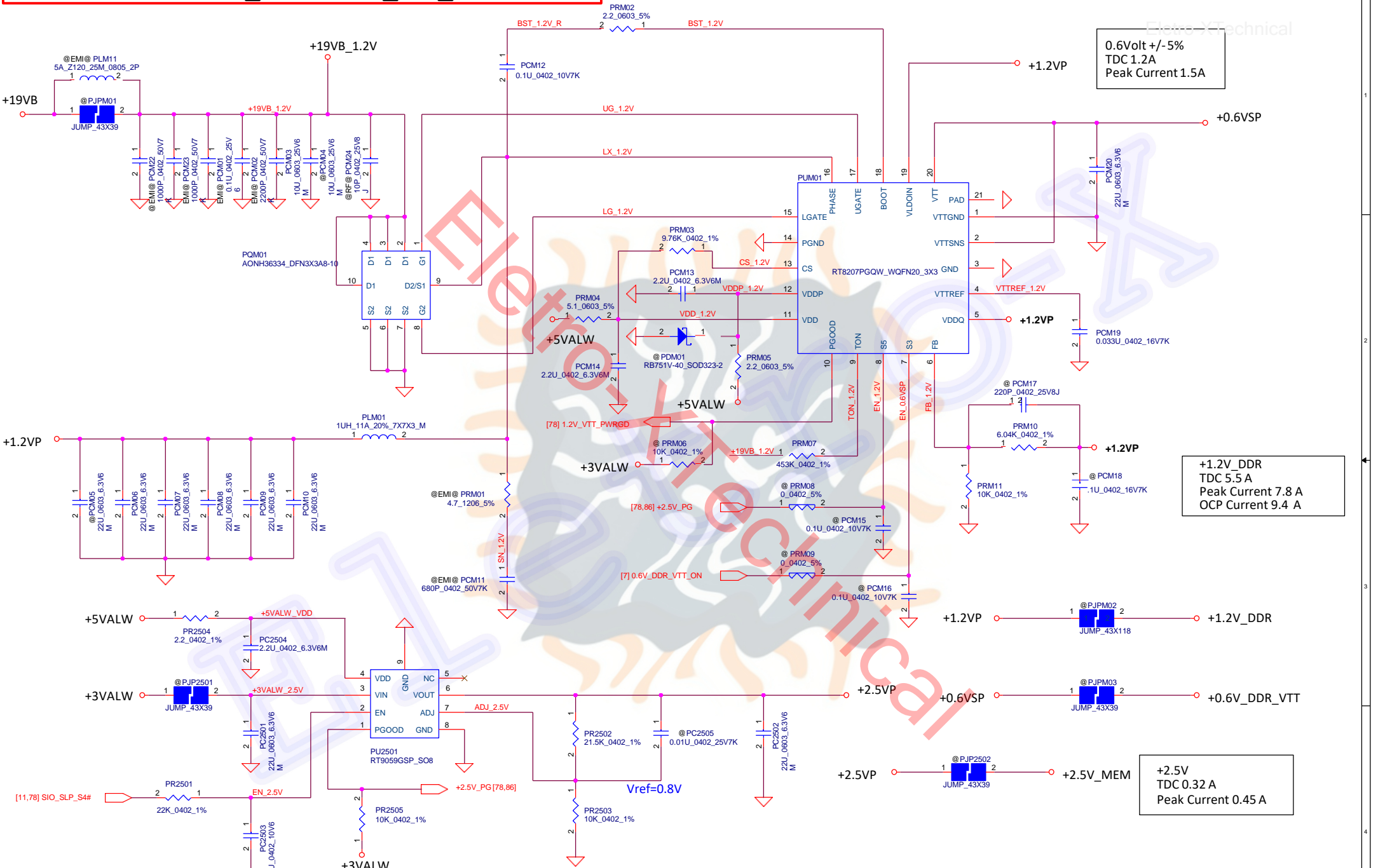
5VALWP  
TDC=6 A  
Peak Current 8 A  
OCP current 10 A

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<b>Compal Electronics, Inc.</b>	
<b>PWR_3.3VALWP/5VALWP</b>	
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**Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT/ +2.5VP**



0.6Volt +/-5%  
TDC 1.2A  
Peak Current 1.5A

+1.2V\_DDR  
TDC 5.5A  
Peak Current 7.8 A  
OCP Current 9.4 A

+2.5V  
TDC 0.32 A  
Peak Current 0.45 A

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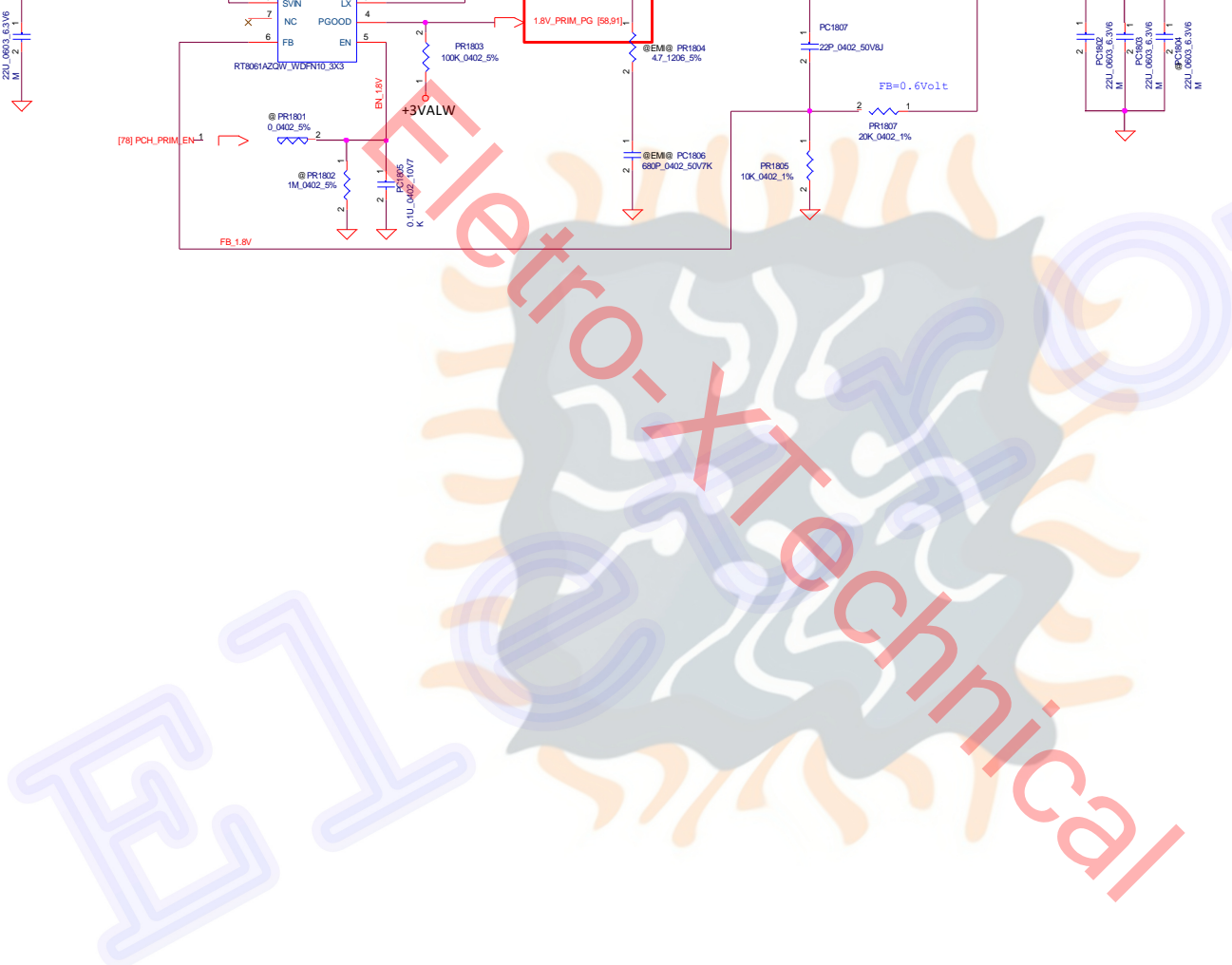
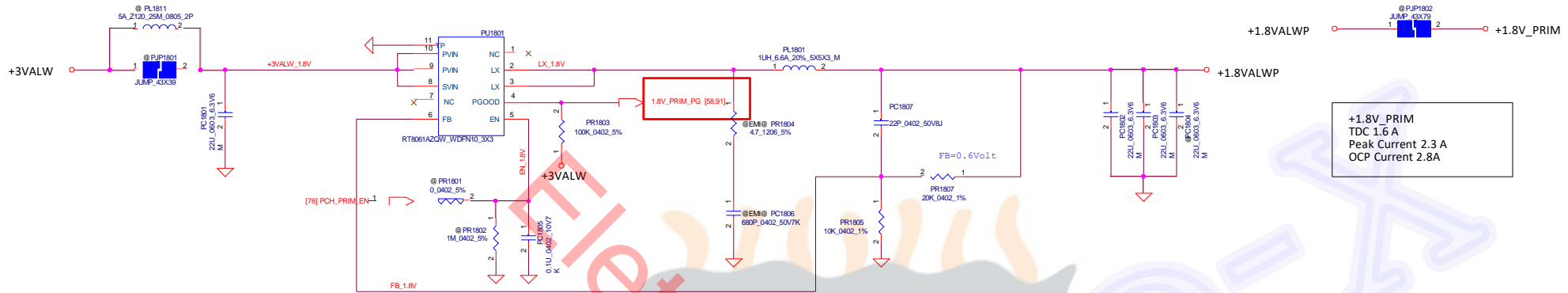
**Compal Electronics, Inc.**

Title: **PWR +1.2V\_MEN/+0.6V/+2.5VP**

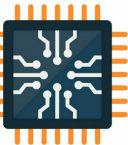
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Date: Monday, July 29, 2019

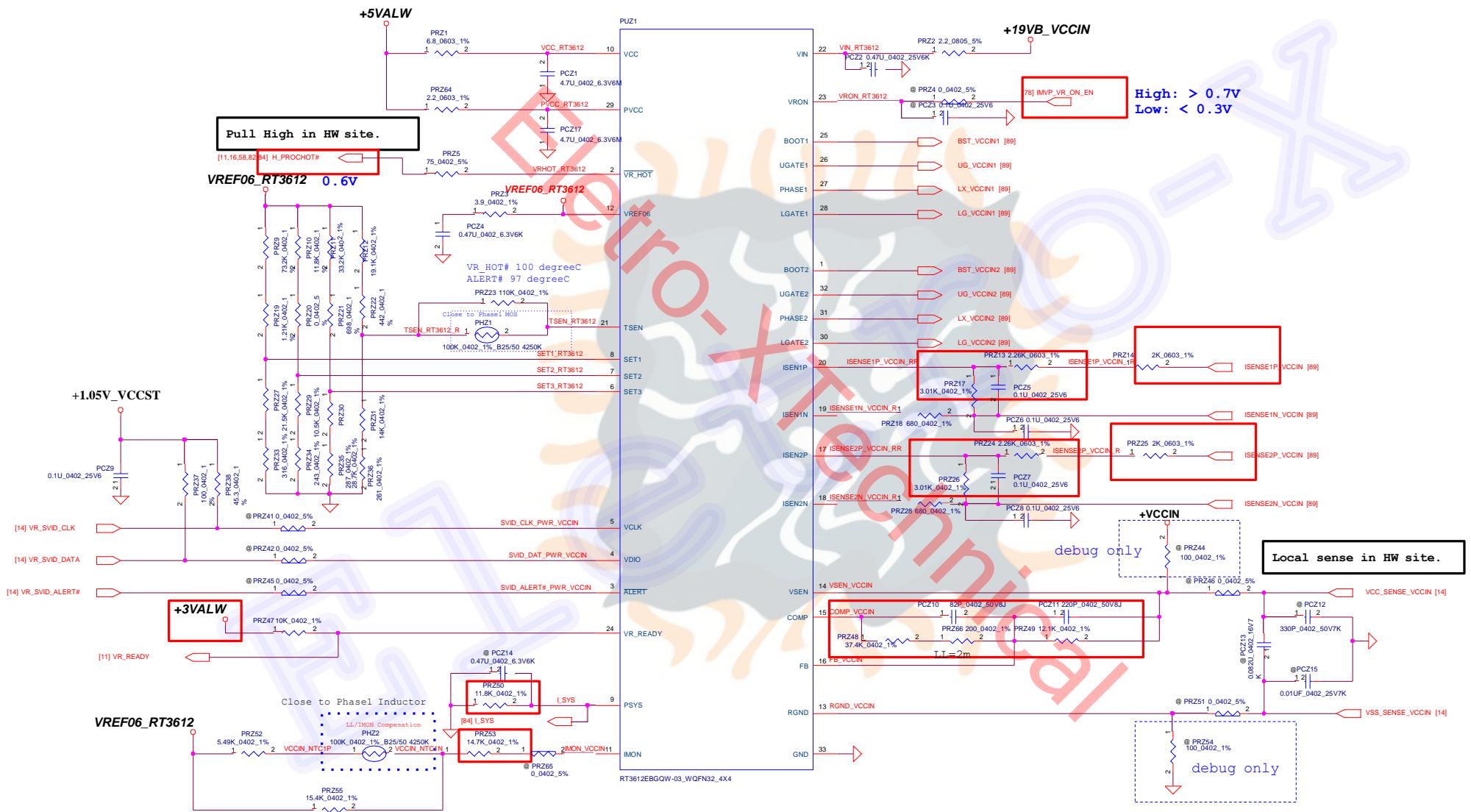
Sheet 86 of 10



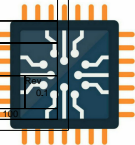
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Date: Monday, July 26, 2019				Sheet 87 of 100



RT3612EBGQW-03

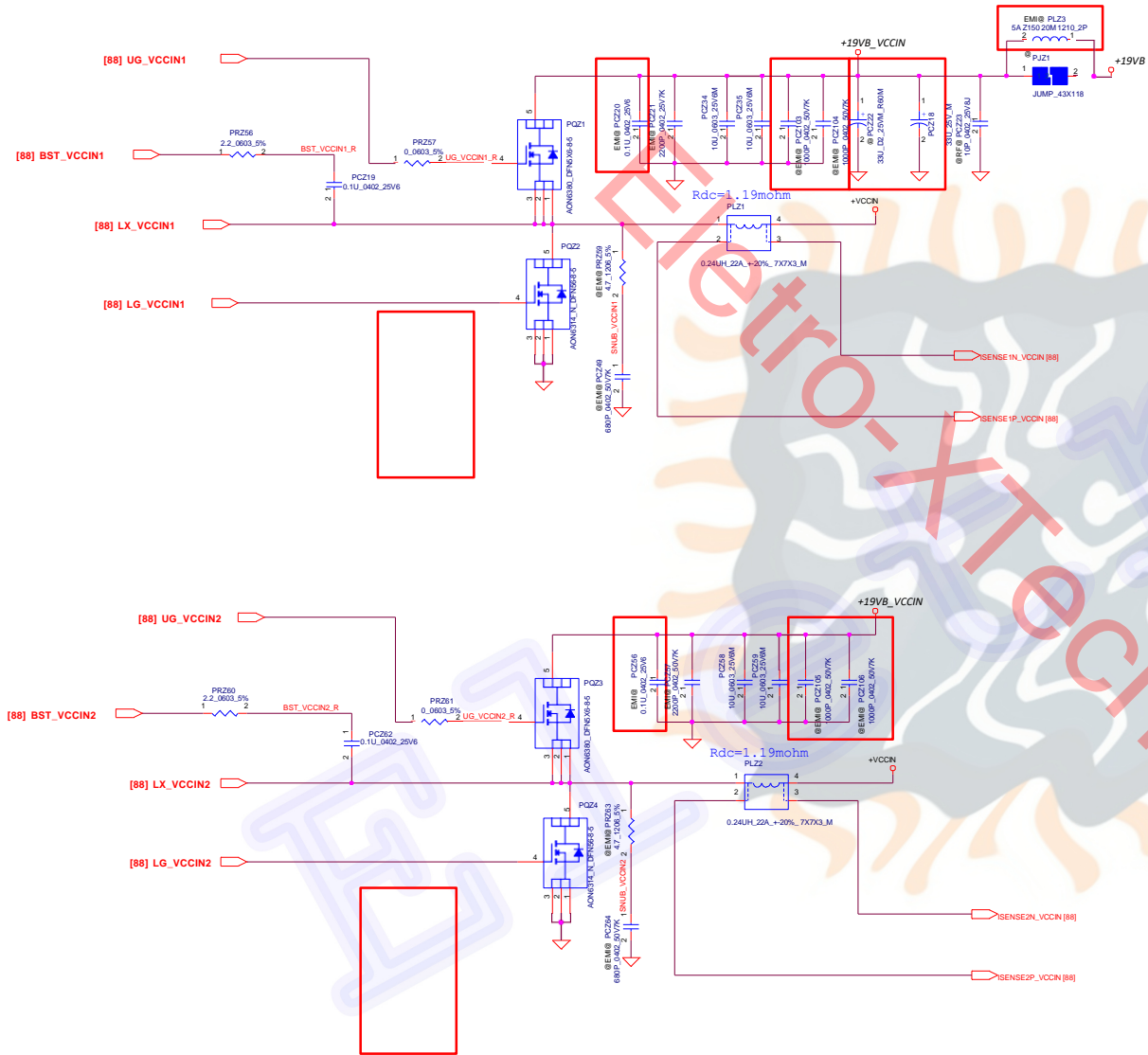


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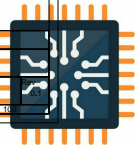


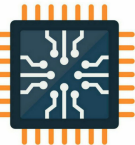
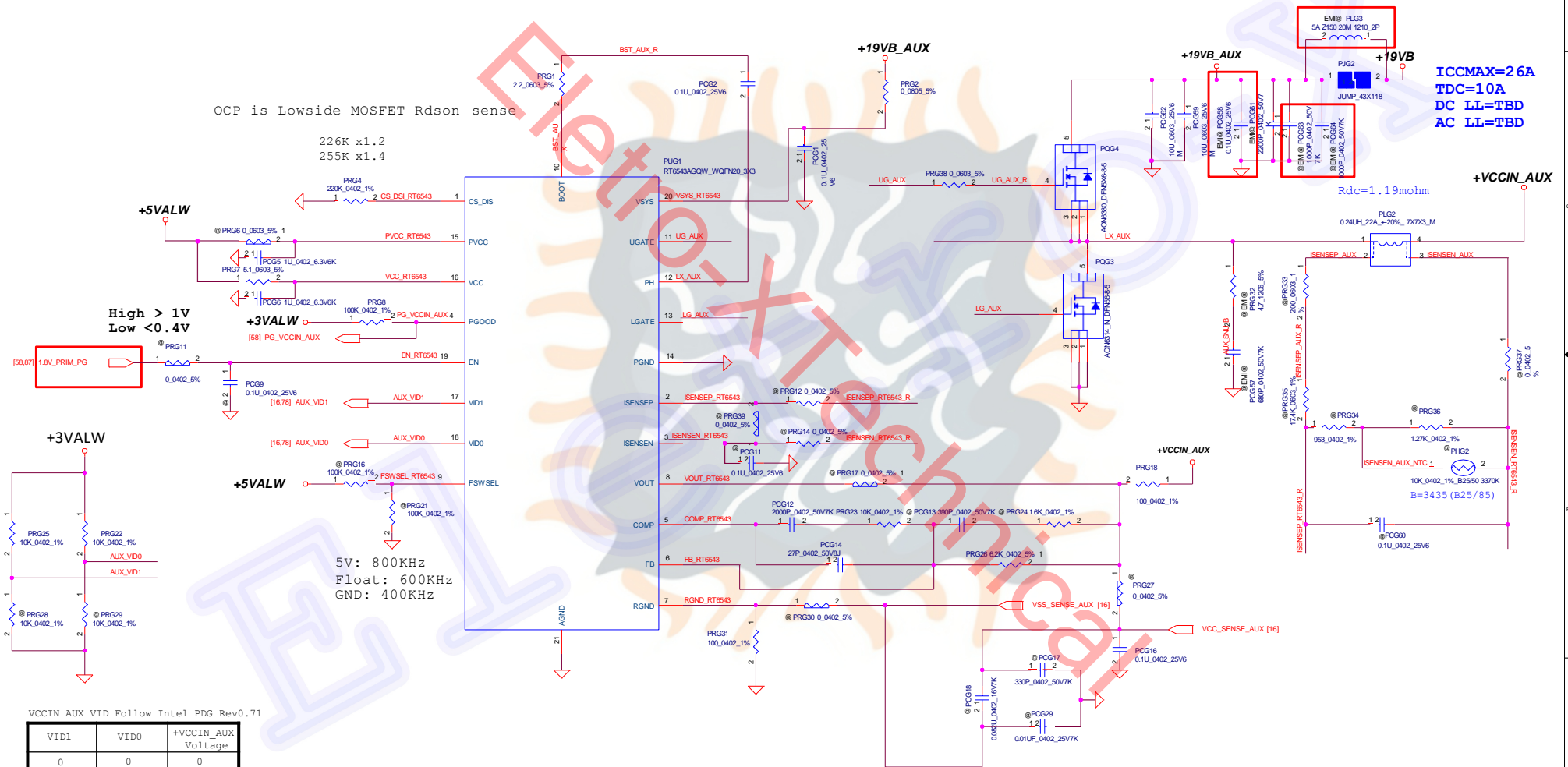
OCP=91  
ICCMAX=70A  
TDC=39A

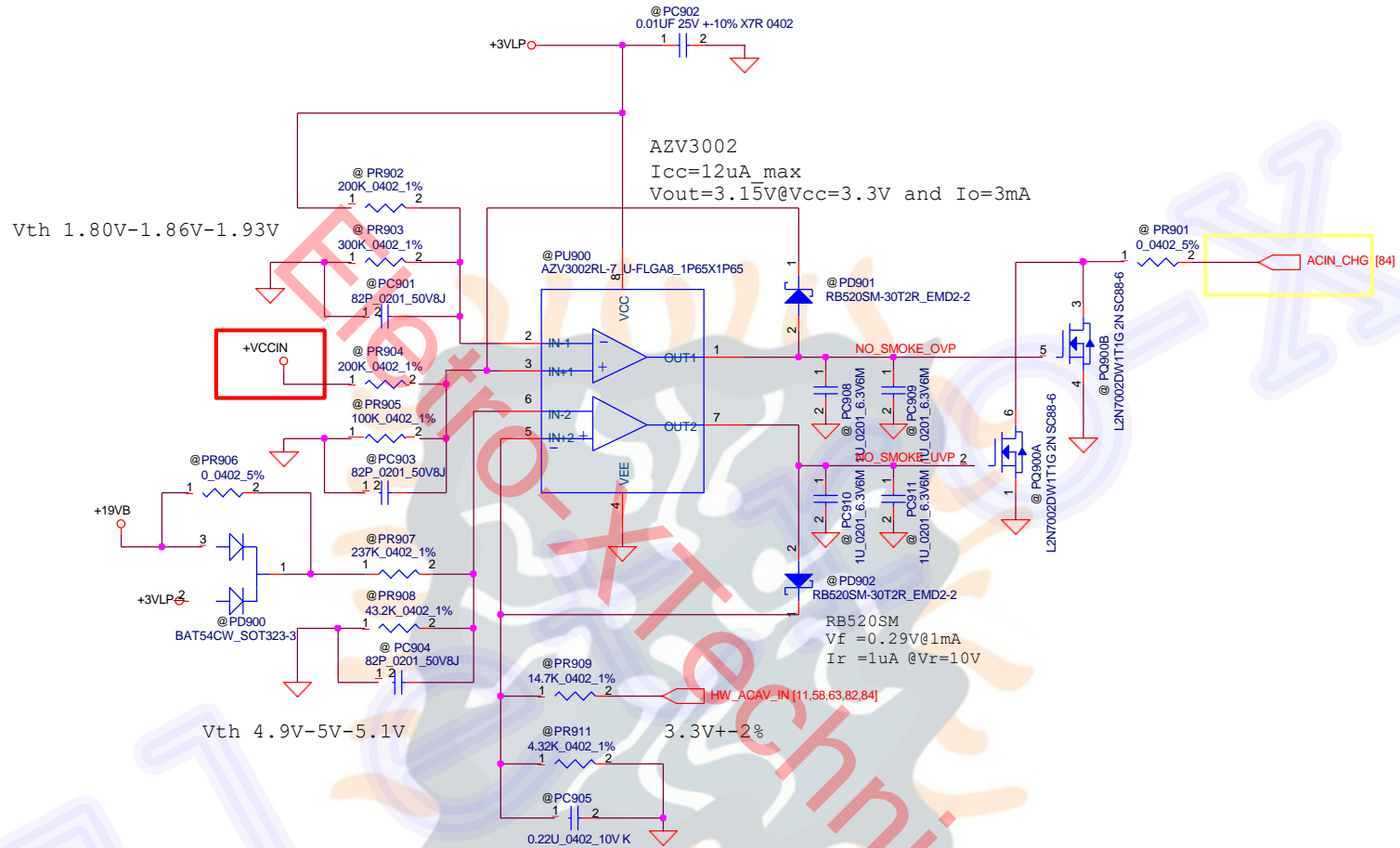
Frequency 600KHz



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<small>Date: Monday, July 25, 2019</small>			<small>Sheet 88 of</small>







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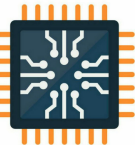


DVT1 EE change list

Design Change									
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout	
<b>Based on 05/15</b>									
1	2018/5/17	8		Add RC207, CPU_SPL_0_CS#1	For 2nd ROM	Y	N	Y	
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ rooting	Y	N	Y	
3	2018/5/17	14		CC52,CC48,CC51,CS change to 0402	meet purchase requirement	Y	Y	Y	
4	2018/5/17	29		CV73-CV78, CV100-CV109 change to 0402	meet purchase requirement	Y	Y	Y	
5	2018/5/17	71		del CU3,CU8 CU4,CU9 IU change to 4.7U	meet purchase requirement	Y	Y	Y	
6	2018/5/20			Del CS6,CU3,CU8; CU13,CU16,CS,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y	
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y	
8	2018/6/4	38		Connect UC1,CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y	
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y	
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183,CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y	
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y	
12	2018/7/4	65		add Rxt10~14	co-lay ST TPM	Y	N	Y	
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y	
14	2018/7/6	65		add Rxt15~RX19	co-lay China TPM	Y	N	Y	

DVT2 EE change list

Design Change									
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout	
<b>Based on 07/16</b>									
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y	
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnect B+	Y	N	Y	
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N	
4		71	RE1	SD034178280=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N	
5			CC54,CC57		fixed 1.05 OVPIBITS382716)	Y	Y	N	
6			U22	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OVPIBITS382716)	Y	Y	N	
7				Remove Typec configuration	Dell PCR	N	Y	N	
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y	
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N	



# Change List ( P. I. R. List )

Eleto-XTechnical

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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1	P83	BATT CONN	20190423	COMPAL	RF request for RF test	Reserve PC16	0.2 (X01)
2	P84	PWR CHARGER	20190423	COMPAL	"Based on Loki G issue, change to follow Renesas recommendation"	<ol style="list-style-type: none"> <li>1. PCB07 change to 0603</li> <li>2. Remove PCB71</li> <li>3. PRB15 change to 1206</li> </ol>	0.2 (X01)
3	P96	NO SMOKE	20190423	COMPAL	customer request	Add page 96: reserve NO SMOKE schematic	0.2 (X01)
4	P88	PWR VCCIN	20190507	COMPAL	Change RC value for Intel EA test	"Change RC value for Intel test: PCZ77=330UF PCZ79/80/81/82/84/85/86/87/90/96/98/99/100/102=22uF VCCAUX Output caps 1+9 PCG46=330UF PCG19/24/28/50/51/65/71/75/76=22uF PRZ14/25=2.21Kohm PRZ13/24=2.05kohm PRZ17/26=3.01Kohm PRZ48=37.4Kohm PRZ66=200ohm PRZ49=12.1Kohm PRZ53=14.7kohm PCZ10=82pF PCZ11=220pF	0.2 (X01)



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